

# Reliability Scaling of Nanoscale Avalanche Photodiodes in High-Speed Optical Communication

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## Abstract

In the present era of big data and 5G wireless, both microelectronic and photonic components are indispensable building blocks. For microelectronics, device miniaturization has been following Moore's law to attain higher speed and greater functionality. For photonics, similar device scaling is also evolving in both lasers and photodiodes to transmit high data rates of 25 Gb/s and beyond. However, such device miniaturization may impose challenges such as reliability and fabrication that require careful scientific and engineering studies. In particular, the reliability understanding of photonic device scaling is fairly rudimentary with only scattered reports. In this paper, we study the device and reliability scaling of nanoscale avalanche photodiodes (APDs). The device miniaturization of APDs mainly involves thickness reduction in the charge control and multiplication layers. The layer reduction however causes an increase in breakdown field that may adversely affect reliability in several aspects such as electrical/optical overload and electrostatic discharge (ESD). We present a new reliability degradation model of APDs based on the breakdown field and correlate it with the experimental data. Empirical reliability equations are instituted to establish quantitative formulation. We discuss the overload and ESD performances as a function of breakdown field for both planar-type and mesa-type APD structures.

**Keywords:** Reliability, Avalanche Photodiode, Optical Communication, Overload, ESD, 5G Wireless

## 1. Introduction

Device scaling is the key driver for the sustained success of lower cost and increased functionality in semiconductor industry (Moore, 1965; Semiconductor Industry Association, 2019; Arden et al., 2010). For microelectronics, the feature size of integrated circuits (ICs) has been following Moore's Law, shrinking from 0.9 $\mu$ m in the early 1990s to 7nm in 2019. Owing to the large market size and broad applications, the IC semiconductor companies have been increasing their R&D spending on research and reliability studies, up to \$58.9 billion in 2017 (IC Insights, 2017). IC Insights projects that semiconductor R&D will rise by a 5.5% compound annual growth rate (CAGR) from 2018 through 2023, up from 3.6% during 2013-2018 (McGrath, 2019). To ensure product quality, experimental and modelling of reliability failure modes related to electromigration, stress migration, dielectric breakdown, hot carrier, soft error, and three-dimensional (3D) ICs have been extensively studied over the past few decades (Oates, 2015; McPherson, 2012; Hu, 2009; Tu, 2011).

On the other hand, nanophotonics has also been through similar miniaturization to achieve ever-increasing speed albeit at much smaller economic scale (Chen et al., 2018; Nada et al., 2012; Huang, 2016). The typical miniaturization involves reduction in critical layer thickness. However, the technology design rule of nanophotonics in general is not as well defined compared to the IC counterpart. Since the device roadmap of photonics is generally not as specific as that of the ICs, the reliability studies are expected to be relatively more sporadic (Huang, 2015; Ishimura et al., 2007; Huang et al., 2018; Kim et al., 2001; Takeshita et al., 2006; Watanabe et al., 1996; Huang et al., 2017; Smith et al., 2009).

In this paper, we study the reliability scaling of nanoscale APD photodetectors. The miniaturization of APD typically involves the thickness reduction of multiplication layer to attain higher device speed. However, the layer thickness reduction would also lead to higher electric field that may impose adverse effects on reliability. We report the reliability data of APDs as a function of breakdown electric field resulting from the miniaturization in the

multiplication layer thickness. We discuss the reliability aspects of optical and electrical overload as well as electrostatic discharge (ESD) from device scaling.

## 2. Experimental

To study the reliability scaling of different APD generations, we compared the reliability performances of 2.5G APD, 10G APD, and 25G APD devices (Huang et al., 2018). The photodetectors for 2.5G data rate are based on planar-type structures because low cost and simple processing are critical for those commercial applications. For 10G and 25G APDs, mesa-type structures are typically needed to achieve the high-speed requirements.

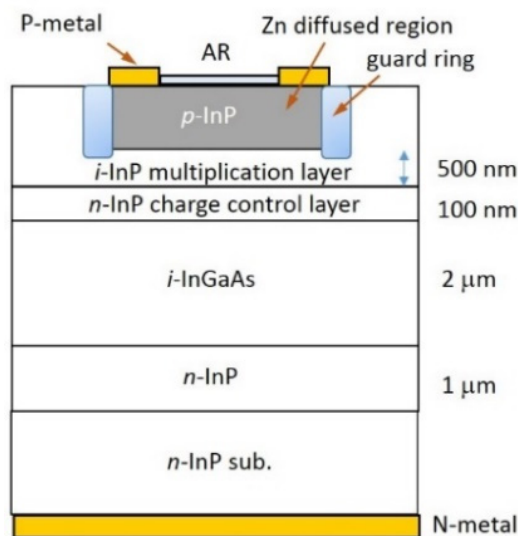


Figure 1. Schematic of the 2.5G APD device based on planar-type structure. The multiplication and charge control layers are 500 and 100nm, respectively

Figure 1 shows the schematic of the 2.5G APD device based on planar-type structure where the p-type and n-type metal contacts are formed on top and bottom of the chip, respectively. The first layer on top is the p-type InP formed by Zn diffusion. Guard ring is formed to avoid the edge breakdown at the p-type InP diffused region (Neitzert et al., 1997). The intrinsic InP layer (~500nm) below the p-type InP serves as the multiplication layer (M-layer). Immediately under the M-layer, a 100nm thick charge control layer of n-type InP is formed. The light absorption occurs in a 2μm intrinsic InGaAs layer. Finally, an n-type InP buffer layer is formed on top of the n-InP substrate.

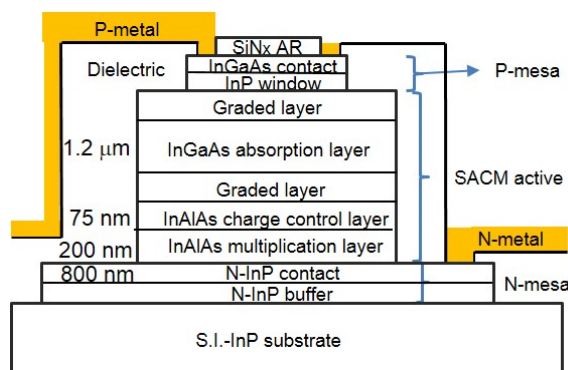


Figure 2. Schematic of the 10G APD device based on mesa-type structure. The multiplication and charge control layers are 200 and 75nm, respectively

Figure 2 shows the schematic of the 10G APD based on mesa structure where the p-type and n-type metal contacts are both on the top of the chip (Huang et al., 2017; Huang et al., 2016). The P-mesa made up of p-type InGaAs

contact and p-type InP window layers is located at the top. The p-contact is usually formed by a metal ring surrounding the circular anti-reflective (AR) window. The p-metal ring is connected to the outside p-pad by a metal bridge. The N-mesa consisting of the n-type InP buffer and n-type contact layers is at the bottom. The active region is designed to be in the middle, consisting of the InGaAs absorption layers (1200nm), InAlAs charge control (75nm), and InAlAs multiplication (200nm). Such active structure is also called separate absorption, charge, and multiplication (SACM). For the passivation, low-k dielectric material such as polyimide is used to reduce the capacitance.

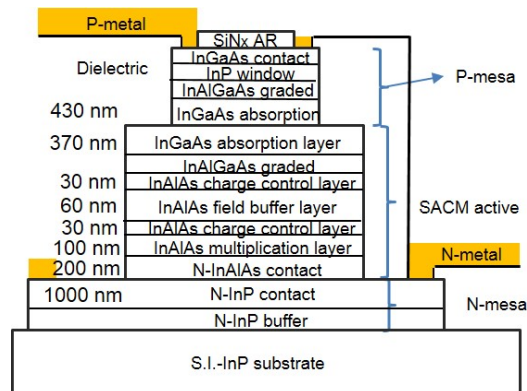


Figure 3. Schematic of the 25G APD device based on mesa-type structure. The multiplication and charge control layers are 100 and 30nm, respectively

Figure 3 shows the schematic of the 25G APD based on mesa structure. In this design, more sophisticated mesa structures such as three mesas and dual charge layers are designed to improve the bandwidth-gain product (Chen et al., 2018; Nada et al., 2012; Wu et al., 2018). The 25G APD structure consists of three mesas with increasing diameter from top to bottom. Similar to 10G APD, the top of 25G APD is comprised of the p-type InGaAs contact layer and p-type InP window layer. To achieve 25G high-speed, thin intrinsic InAlAs multiplication (100nm) and InAlAs dual charge (30nm each) layers are employed. For the InGaAs absorption layer, the top 470nm portion is etched to form the topmost mesa structure, and the remaining 370nm portion in the middle mesa structure. In addition, the partially depleted p-type absorber, which has a graded doping profile (from  $5 \times 10^{19}$  to  $1 \times 10^{17} \text{cm}^{-3}$ , top to bottom) is used to shorten the hole transit time and to accelerate the electron diffusion process (Nada et al., 2012). The thickness of the InGaAs absorption layer is also designed to be thinner ( $\sim 0.8 \mu\text{m}$ ).

### 3. Results and Discussion

Figure 4 shows the general internal electric field profile of an APD device (Huang et al., 2017). The electric field is typically low in the absorption layer. The field is increasing in the charge layer and reaches the maximum in the multiplication layer that is responsible for avalanche breakdown operation (Campbell, 2016). The doping of the InAlAs charge control layer can affect the relative field strength between the absorption and multiplication regions. At the breakdown voltage for avalanche operation, the voltage drop is roughly divided at the absorption and multiplication layers. Since the absorption layer is very thick, the electric field of the absorber is usually low enough to prevent breakdown. Due to the thin layer, the electric field is much higher in the multiplication layer. Assuming half of the voltage drop is across the multiplication layer, we can estimate the breakdown electric field at the multiplication layer (Saleh et al., 2001). Our previous study showed that the breakdown fields in the multiplication layers for 2.5G, 10G, and 25G APDs were about 560, 800, and 1300kV/cm, respectively (Huang et al., 2017).

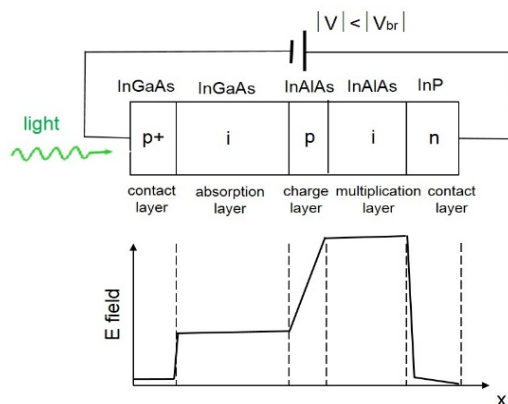


Figure 4. Schematic of internal electric field profile of the APD structure corresponding to the InGaAs absorption, the InAlAs charge control, and the multiplication layers

Since the breakdown electric field is the maximum at the multiplication layer, we expect that this layer may become the weak spot when exposing to the harsh environmental stresses. In the following section, we attempt to correlate the breakdown electric field with reliability performance. We experimentally measure and compare the three types of APDs (2.5G, 10G, and 25G). We present a new reliability degradation model of APDs based on the breakdown field and correlate it with the experimental data. We discuss the electrical/optical overload and electrostatic discharge performances as a function of breakdown field. Empirical reliability equations are instituted to establish quantitative formulation. We also compare the difference between mesa-type and planar-type APD structures.

### 3.1 Optical/Electrical Overload

In order to verify the photodetector’s robustness against simultaneous electrical and optical stresses, the APD devices were tested with overload stress in continuous-wave (CW) mode, as illustrated in Figure 5. For each type of APD, six devices were tested to establish statistical box plot distribution. To determine the damage threshold of overload, the optical stress was ramped up from -4 to +4 dBm incrementally until the device shows failure with the dark current greater than 100 nA.

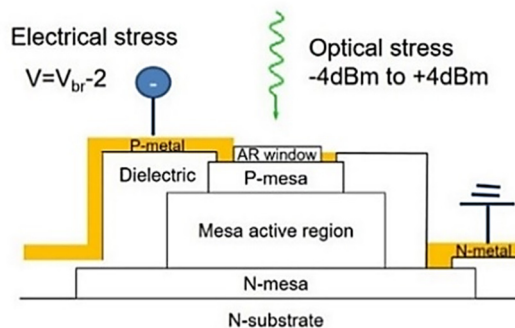


Figure 5. Schematic of APD setup for CW overload stress. The APD chip was exposed to both electrical and optical stresses

Figure 6 shows the CW-mode overload damage threshold of APDs as a function of breakdown electric field. There are several interesting observations worth mentioning. First, the overload damage threshold generally decreases with increasing breakdown electric field. As the device speed increases, the overload threshold decreases as a result of higher electric field. Second, the 2.5G APD of planar-type structure exhibits higher damage threshold than that of the regression line extrapolated from the mesa-type. The superior overload performance of the planar-type may be attributed to the reduction in surface defects since the planar structure does not involve any mesa etch (Kim et al., 2001; Takeshita et al., 2006; Watanabe et al., 1996; Huang et al., 2016).

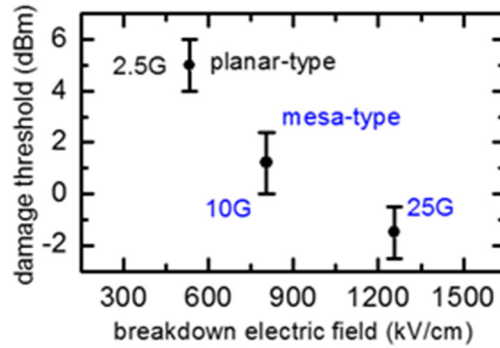


Figure 6. CW overload of APD as a function of breakdown electric field

The overload threshold of APD can be expressed in Equation (1) where  $P_t$  is the overload damage threshold,  $B$  is a constant depending on the planar-type or mesa-type,  $E_{br}$  is the breakdown electric field, and  $\alpha$  is the exponent of overload threshold.

$$P_t = B E_{br}^{-\alpha} \tag{1}$$

By taking the natural logarithm, Equation (1) can be expanded into Equation (2) where the exponent can be determined by the coefficient of the second term. To estimate  $B$  and  $\alpha$ , we assume that the three APD devices follow the same exponent  $\alpha$  with different constant  $B$  depending on the planar and mesa structures. By taking the slope of the fitting line between the 10G and 25G APD data, the value of  $\alpha$  is estimated to be about 1.42. Once the exponent is determined, we can then determine the constant  $B$ . The values of  $B$  are estimated to be 25260 and 16676 for the planar-type and mesa-type, respectively. Figure 7 shows the modelling curves overlaid with the experimental overload data of the three APD devices in our study. The modelling based on Equation (1) provides a good empirical description of the overload as a function of breakdown field for both planar-type and mesa-type APD devices.

$$\ln(P_t) = \ln(B) - \alpha \ln(E_{br}) \tag{2}$$

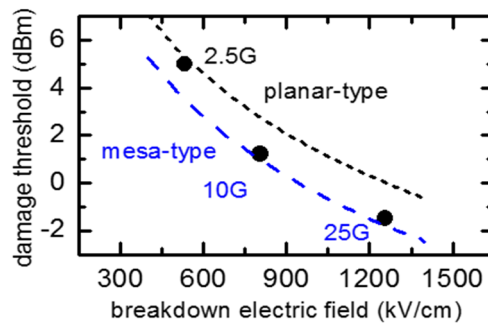


Figure 7. Modelling vs. experimental overload of APDs as a function of breakdown electric field. The modelling curves are based on Equation (1) where the planar-type and mesa-type are fitted with different values of constant  $B$

### 3.2 ESD

Figure 8 shows the ESD test setup with a human-body-model (HBM) simulator consisting of a circuit of 1.5k $\Omega$  and 100pF. For each type of APD, six devices were tested to establish statistical box plot distribution. The HBM-test method was in adherence to Telcordia TR-NWT-000870 (Bellcore, 1991). The APD chip was attached to submount in the transistor outline (TO) package. The electrical leads of cathode and anode were connected to the ESD tester. The ground of the ESD tester was connected to the n-side (cathode) of the APD, whereas the ESD pulse was applied to the p-side (anode). The ESD stress voltage started from 0.1kV and ramped successively up until the ESD failure occurs. Current versus voltage (IV) curve was recorded before and after each ESD stress to determine the ESD-failure threshold (Huang et al., 2016; Huang et al., 2007; Huang et al., 2019). The ESD failure was defined as the dark current greater than 100nA.

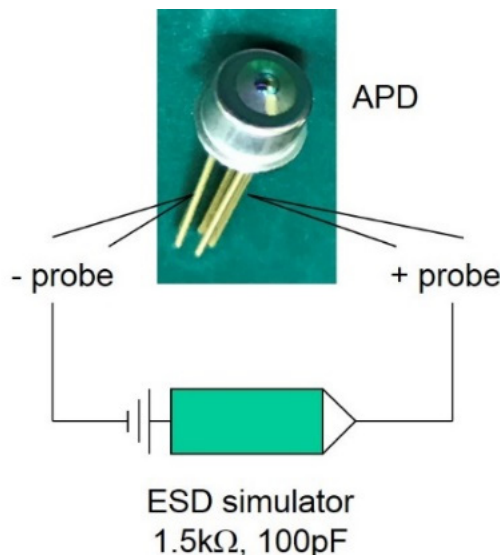


Figure 8. Schematic of APD on TO for ESD test. The APD chip was connected to ESD simulator. The ESD stress started at low level and ramped up incrementally until failure occurred

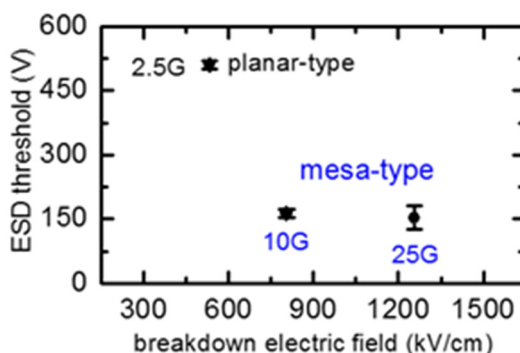


Figure 9. ESD damage threshold of APD as a function of breakdown electric field

Figure 9 shows the reverse ESD threshold of APD as a function of breakdown electric field. Again, the reverse ESD threshold generally decreases with increasing breakdown electric field. As the device speed increases, the ESD threshold decreases as a result of higher electric field. The other similar trend is that the 2.5G APD of planar-type structure exhibits higher damage threshold than what’s expected from the mesa-type, likely related to the absence of surface defects from mesa etch.

The reverse ESD threshold of APD can be expressed in Equation (3) where  $R_v$  is the reverse ESD threshold,  $C$  is a constant depending on the planar-type or mesa-type, and  $\beta$  is the exponent of ESD damage threshold.

$$R_v = C E_{br}^{-\beta} \tag{3}$$

Equation (3) can be rewritten in the form of natural logarithm as shown in Equation (4). The exponent can be determined by the slope of Figure 5.

$$\ln(R_v) = \ln(C) - \beta \ln(E_{br}) \tag{4}$$

Again, we assume that the three APD devices follow the same exponent  $\beta$  and the planar-type exhibits different constant  $C$  compared to the mesa-type. By taking the slope of the fitting line between the 10G and 25G APD data, the value of  $\beta$  is estimated to be about 0.25. The values of constant  $C$  are estimated to be 2432 and 798 for the planar-type and mesa-type, respectively. Figure 10 shows the modelling and experimental ESD thresholds as a function of breakdown field for the three APD devices. The modelling based on Equation (3) gives a good account of the ESD threshold versus breakdown field for both planar-type and mesa-type APD devices.

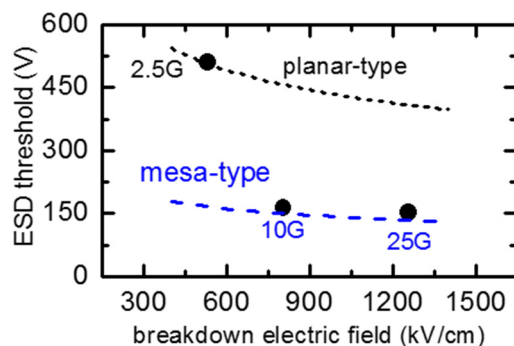


Figure 10. Modelling vs. experimental ESD threshold of APDs as a function of breakdown electric field. The modelling curves are based on Equation (3) where the planar-type and mesa-type are fitted with different values of constant C

#### 4. Conclusion

We have studied the device scaling effect of nanoscale APD devices on several reliability aspects including optical/electrical overload and ESD. We have shown the experimental correlation between the breakdown electric field and reliability for the 2.5G, 10G, and 25G APD devices. In general, the damage threshold tends to decrease with increasing breakdown electric field in the multiplication layer. To account for the experimental data, we have instituted reliability models as a function of APD breakdown field and deduced the exponent for optical/electrical overload and ESD. Based on the fitting to the experimental data, the exponents of overload and ESD are estimated to be 1.42 and 0.25, respectively. The modelling provides a good empirical description of overload and ESD as a function of breakdown field for both planar-type and mesa-type APDs. With the proper fitting constants, the modelling curves show good agreement with the experimental data and offer good predictions of damage threshold versus breakdown field.

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#### Conflict of interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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