



Design and Applications of Integrated Transducers in Commercial CMOS Technology

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Monolithic integration of Microelectromechanical Systems (MEMS) directly within CMOS technology offers enhanced functionality for integrated circuits (IC) and the potential improvement of system-level performance for MEMS devices in close proximity to biasing and sense circuits. While the bulk of CMOS-MEMS solutions involve post-processing of CMOS chips to define freely-suspended MEMS structures, there are key applications and conditions under which a solid, unreleased acoustic structure composed of the CMOS stack is preferred. Unreleased CMOS-MEMS devices benefit from lower barrier-to-entry with no post-processing of the CMOS chip, simplified packaging, robustness under acceleration and shock, stress gradient insensitivity, and opportunities for frequency scaling. This paper provides a review of advances in unreleased CMOS-MEMS devices over the past decade, with focus on dispersion engineering of guided waves in CMOS, acoustic confinement, CMOS-MEMS transducers, and large signal modeling. We discuss performance limits with standard capacitive transduction, with emphasis on performance boost with emerging CMOS materials including ferroelectrics under development for memory.

Keywords: CMOS-MEMS resonator, ferroelectric, transducer, phononic crystal (PnC), acoustic waveguide

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2 INTRODUCTION

Traditional MEMS transducer-based Surface and Bulk Acoustic Wave (SAW and BAW) technology has revolutionized the telecommunications sector over the past two decades, at present enabling the integration of more than a 100 high-performance filters into a handheld device (Ruby, 2015; Hagelauer et al., 2018). Likewise, CMOS-integrated MEMS transducers promise an enabling technology in multiple domains, including clock generation and routing (Srivastava et al., 2021a), chip security (Willers et al., 2016), oscillatory computing (Mahboob and Yamaguchi, 2008; Mahboob et al., 2011; Nikonov et al., 2015; Jackson et al., 2018; Romera et al., 2018; Corti et al., 2021), and adaptive filters for next-generation radio communication (He et al., 2020) because of their inherent size, weight, and power (SWaP) advantages together with the ease of impedance matching and reduced electrical parasitics.

While MEMS transducers are most commonly integrated with CMOS at the PCB or package level, monolithic integration into standard CMOS processes has been a longtime research effort (Fedder et al., 2008). The primary drawback of MEMS-first and MEMS-last approaches is the increased implementation cost due to added process complexity. This paper reviews an alternate approach to integration of unreleased CMOS-MEMS devices in commercial processes without the need for post-CMOS fabrication steps to freely suspend mechanical structures. Additional advantages of unreleased implementations include reduced acceleration sensitivity and lowered susceptibility to reliability concerns arising out of chip

TABLE 1 | Comparison of CMOS-MEMS designs implemented in different process technologies.

Design	Process	Resonance frequency (GHz)	Resonance mode	Transduction mechanisms	Q-factor	Transduction efficiency
Weinstein and Bhawe, (2010a)	Custom	11.72	Length Extensional	Capacitive Drive Transistor Sense	1831	$g_{m,mech} = 22 \mu\text{S}$
Weinstein and Bhawe, (2010b)	Custom	37.1	Length Extensional	Capacitive Drive Transistor Sense	560	$g_{m,mech} = 35 \mu\text{S}$
Marathe et al. (2012)	IBM12RF SOI Planar	11.54	FEOL Cavity	Capacitive Drive Transistor Sense	24	$g_{m,mech} = 37.5 \mu\text{S}$
Bahr et al. (2015)	IBM12RF SOI Planar	2.81	FEOL Cavity	Capacitive Drive Transistor Sense	252	$g_{m,mech} = 0.56 \mu\text{S}$
Bahr and Weinstein, (2016)	IBM12RF SOI Planar	3.19	FEOL Waveguided	Capacitive Drive Transistor Sense	13,300	$g_{m,mech} = 0.14 \mu\text{S}$
Anderson et al. (2021)	GF 14 nm FinFET	11.7	FEOL Waveguided	Capacitive Drive Transistor Sense	69.8	$g_{m,mech} = 4.49 \mu\text{S}$
He et al. (2020)	TI HPE035 FeRAM	0.703	BEOL Waveguided	Piezoelectric Drive and Sense	1,012	$k_{eff}^2 = 0.047\%$

The $g_{m,mech}$ represents the electromechanical transconductance of transistor sensed RBT designs and k_{eff}^2 is the effective coupling coefficient (He et al., 2020).

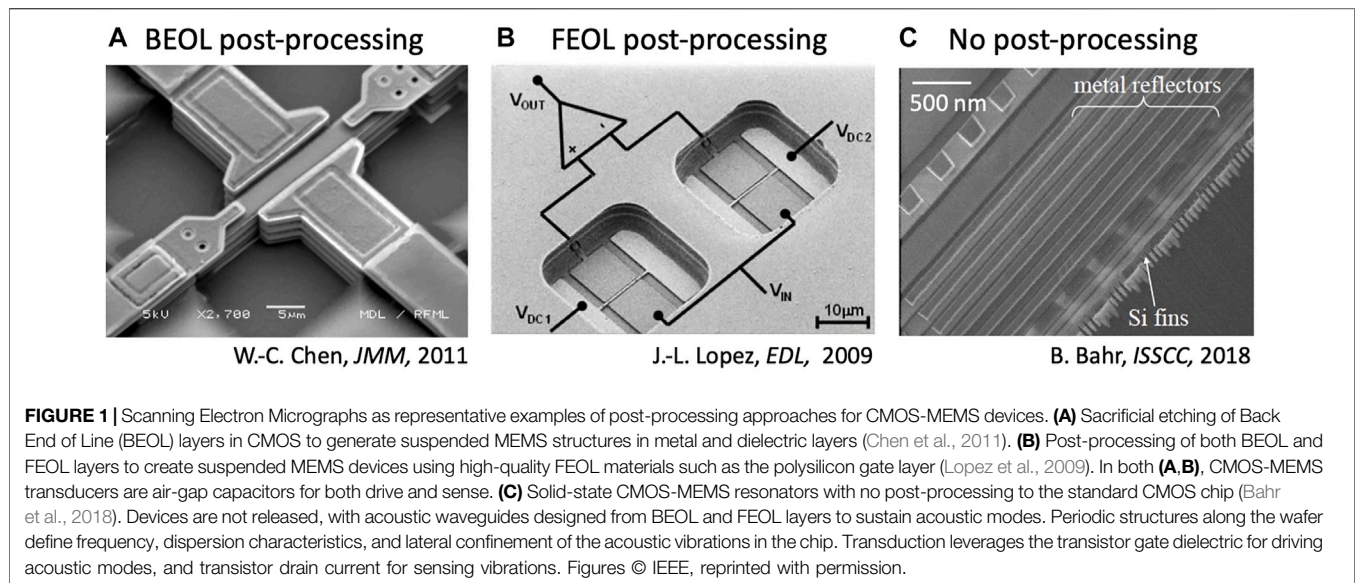
dicing and packaging operations (Ivira et al., 2006). This has been demonstrated for unreleased devices such as Solidly Mounted Resonators (SMRs) (Birdsall et al., 2002) and SAW resonators (Tiersten et al., 1986) which exhibit acceleration sensitivities in the 1–2 ppb/g range as compared to released Film Bulk Acoustic Resonator (FBAR) devices which can have sensitivities up to 80 ppb/g (Ruby et al., 2012). Thus far, unreleased CMOS-MEMS devices have included resonant body transistors (RBTs) in the front end of line (FEOL) of IBM12RF 32 nm SOI (Marathe et al., 2014) and GlobalFoundries 14LPP processes (Anderson et al., 2021; Rawat et al., 2022), as well as back end of line (BEOL) resonators in Texas Instruments' HPE035 130 nm FeRAM process (He et al., 2019; He et al., 2020). **Table 1** briefly compares the implementation details and performance parameters of these different CMOS-MEMS designs, which are depicted with traditional MEMS integration approaches in **Figure 1**. This set of devices exemplify the range of frequencies and performance which can be designed for across different technology nodes.

These devices utilize internal dielectric transduction (Weinstein and Bhawe, 2007; Weinstein and Bhawe, 2009) arising out of FEOL gate-oxide capacitance (Marathe et al., 2012) or piezoelectric transduction based on BEOL (He et al., 2019) ferroelectric materials for actuation of the resonance cavity. Sensing of the resonant mode in the same manner as actuation, can also be done capacitively or piezoelectrically. However, the high capacitive feedthrough in the former makes it prohibitively difficult to incorporate. In such cases, a novel resonant sensing scheme enabled by CMOS integration can be utilized, which involves modulation in the electrical characteristics of a sense transistor embedded within the resonant cavity. In this active sensing technique, the periodic stress/strain induces changes to the electronic bandstructure of the channel material resulting in the superposition of a time varying current over the bias current which can then be read out. Carefully engineered modal stress/strain field localization in the transistor channel region and related intricacies for active sensing will be extensively

discussed. In devices based on BEOL-integrated ferroelectrics, piezoelectric drive as well as sense transduction are employed due to higher transduction efficiency of the piezoelectric transduction.

A challenging aspect of integrated CMOS-MEMS devices beyond drive and sense transduction, is the design of a low-loss acoustic resonance cavity which is of paramount importance as far as the overall device Q-factor (key performance parameter) is concerned. First generation RBT devices (Marathe et al., 2012) utilized Acoustic Bragg Reflectors (ABRs) in the longitudinal resonance direction to attain mode localization but the absence of confinement in the BEOL and substrate region resulted in low Q values. A more efficient technique of designing and utilizing a BEOL phononic crystal with a bandgap centered around the mode of interest was employed in the second generation of CMOS-MEMS RBTs (Bahr et al., 2015) which resulted in a 10× Q improvement over the previous generation of devices. The challenge of this approach is that such a structure may be limited by design rule constraints, requiring co-optimization of confinement and resonator design (Bahr et al., 2015; Bahr et al., 2016a). In the latest generation of CMOS-MEMS RBTs (Bahr et al., 2018; Anderson et al., 2021), a phononic waveguiding based approach is used as opposed to separate design of cavity and confinement structures. Acoustic dispersion engineering based design leads to confinement in the BEOL region through PnCs/plate reflectors, in the substrate region through the phenomenon of index guiding and in the lateral periodicity direction through lattice constant mismatch resulting in up to 56× increase in the Q-factor. The same phononic waveguiding approach was also used to design BEOL ferroelectric capacitor based CMOS-MEMS resonators. A comprehensive comparison of different performance metrics of these device across different technologies and operating conditions will also be provided in the paper.

The complexity of commercial processes with their multitude of materials, layers, and geometries means that it is often prohibitive to simulate an entire resonator structure in 3D. Owing to this reason and the differential phononic waveguide based design, it becomes necessary to design such devices



primarily based on a unit cell of the structure with periodic boundary conditions. The discrepancies arising out of these simulation conditions are addressed here with reference to measured device characteristics. The avenues available to the designer in subsequent design iterations to mitigate performance impacts due to variations caused by manufacturing, differing material properties, metal fill and other sources is also discussed. Current devices with internal dielectric transduction tend to use significantly higher number of drive unit cells than sense, with the sense units at the center of the structure where the periodic boundary assumptions are most valid. At the lateral ends of the cavity, both gradual (adiabatic) and abrupt terminations have been studied, with gradual terminations shown to moderately boost Q (Joannopoulos et al., 2008; Anderson et al., 2021). The choice of termination for the cavity may have a large impact in the location and magnitude of spurious modes, again requiring careful consideration by the designer.

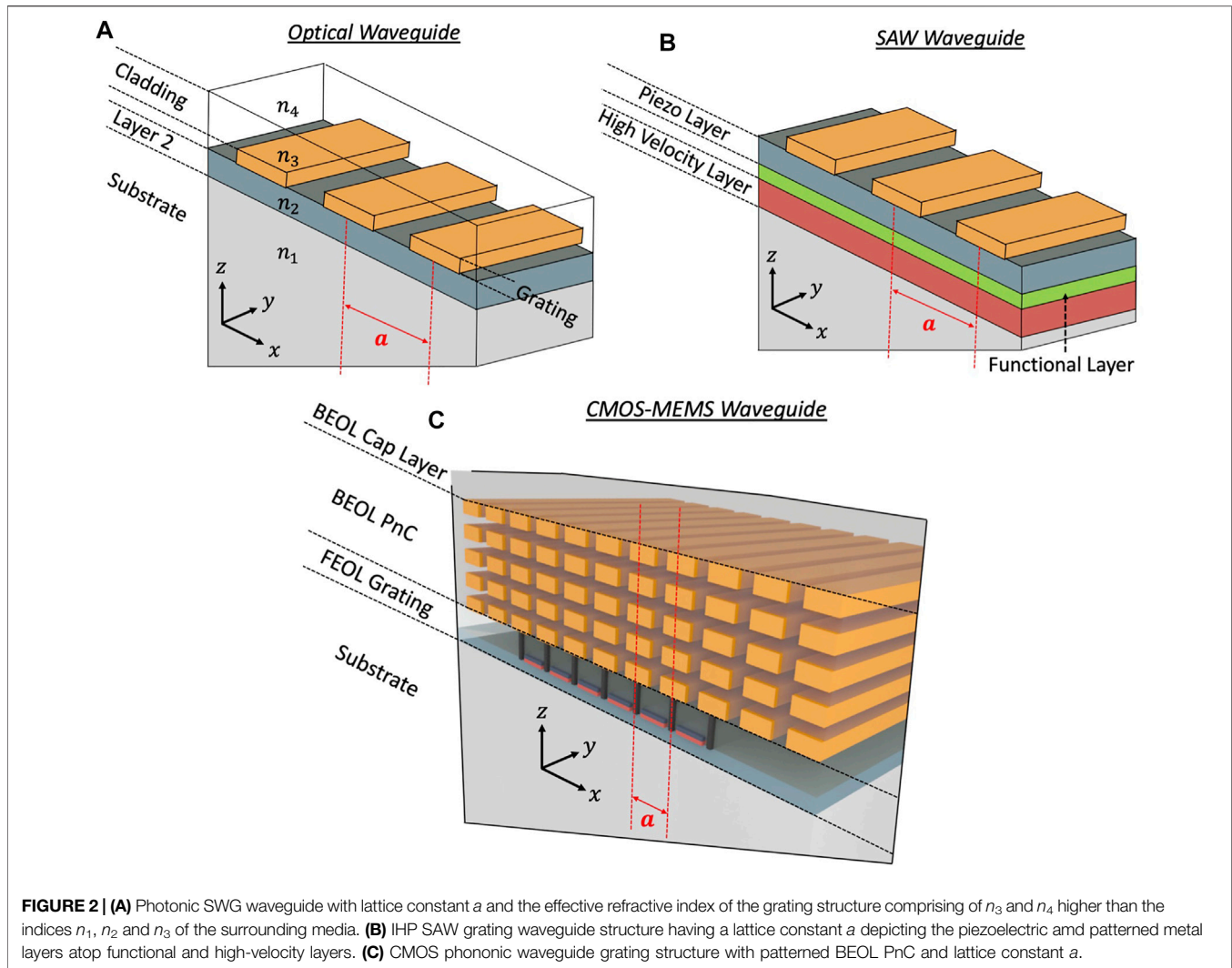
To enable system-level design for different applications of these integrated CMOS-MEMS devices, accurate modeling is a necessity. Initial models employed the modified Butterworth-van-Dyke (MBVD) model to represent the drive transducers and the resonant cavity and controlled current sources for active transistor sensing (Bahr, 2016a). Since these models are small-signal in nature, they are not suitable for use in oscillator applications where large signal swings are encountered. Subsequent device compact models (Bahr et al., 2016b; Bahr et al., 2016c) captured the relevant physics appropriately but were based on theoretical formulations which are not applicable to the complex structures and mode shapes exhibited in the most advanced CMOS-MEMS RBTs. An experimentally-backed, all-encompassing compact model has been developed (Rawat et al., 2022) for this class of CMOS-MEMS devices which can be used for all system-level design scenarios. Detailed modeling aspects of integrated CMOS-MEMS devices are also presented in this paper.

While these CMOS-integrated transducers have been demonstrated in several technology nodes, none have yet

taken advantage of recent advances in CMOS-compatible ferroelectric materials. The integration of doped HfO_2 films into commercial processes brings with it the promise of more efficient piezoelectric actuation (Trentzsch et al., 2016; Hakim et al., 2021), potentially reducing the power and size requirements for CMOS-integrated resonators even further. Other such potential opportunities for performance enhancement as well as new applications are also discussed.

3 GRATED CMOS PHONONIC WAVEGUIDE RESONATOR DESIGN

In the optical domain, devices based on photonic sub-wavelength gratings (SWG) exhibit lower propagation loss than their strip waveguide counterparts, alongside demonstration of tuning of macroscopic optical properties such as refractive index in various material platforms (Rosenblatt et al., 1997; Wang et al., 2016; Kazanskiy et al., 2020; Donzella et al., 2015; Wang et al., 2014; Bock et al., 2010; Cheben et al., 2010). These devices are comprised of lithographically-defined periodic slow-wave structures using two distinct materials with a lattice constant smaller than the wavelength of light. The periodic medium has a higher effective refractive index and is bounded by the lower refractive index substrate below and cladding materials on either side as shown in **Figure 2A**. Owing to this refractive index profile along the z -direction, an optical mode is capable of being completely confined within the grating structure, an extensively investigated phenomenon known as index guiding. Optical couplers, wavelength multiplexers and filters have been demonstrated using this design principle. The acoustic/phononic analogue of index guiding can be seen in certain Sezawa and Love wave based SAW devices such as those in (Takai et al., 2017; Nakagawa et al., 2019), comprised of metal electrode gratings on a piezoelectric layer atop a higher acoustic velocity layer. The SAW mode is vertically confined in the piezoelectric layer with low bulk



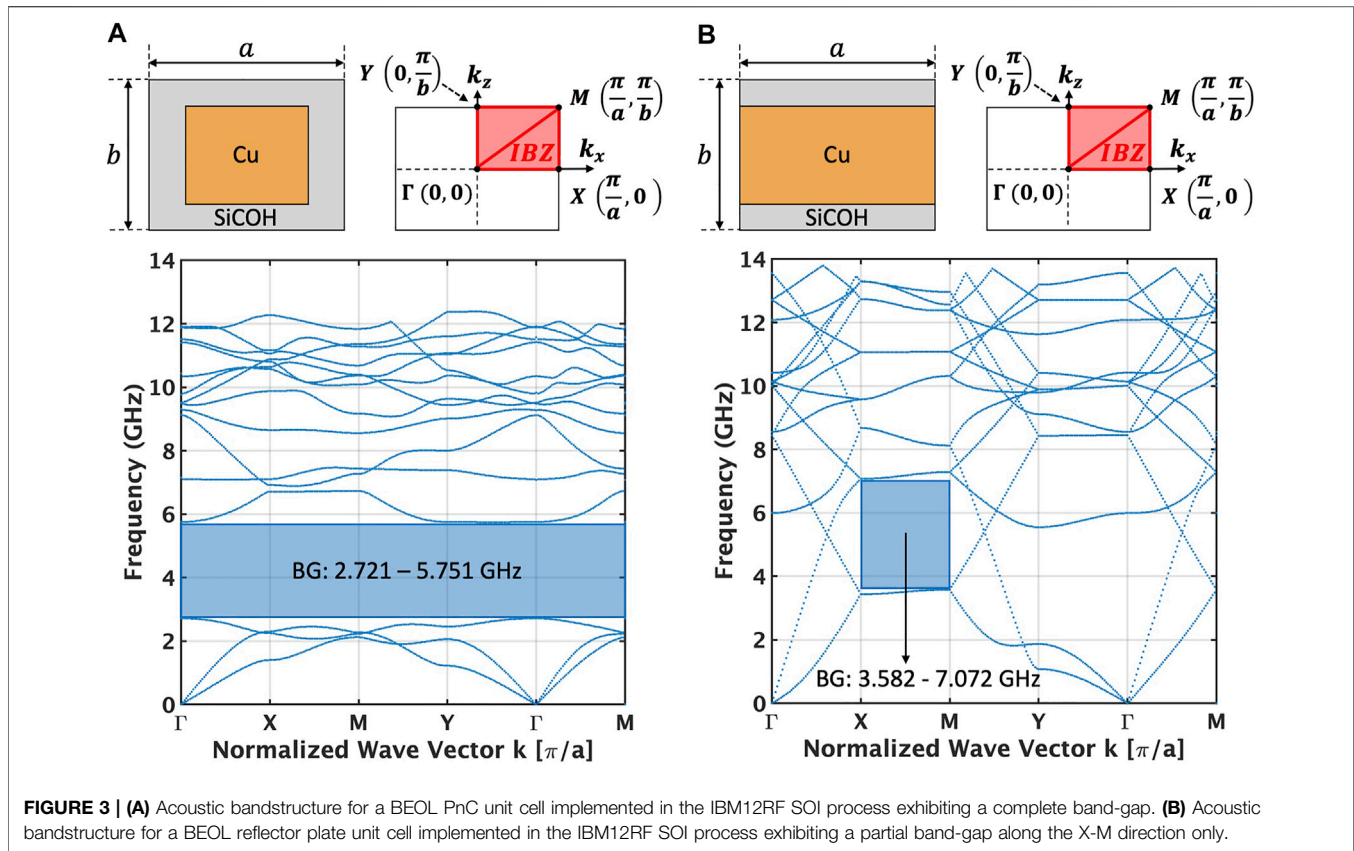
radiative losses due to index guiding resulting in significant improvement in propagation loss relative to unguided SAW modes in bulk piezoelectric substrates.

Toward the goal of acoustic wave propagation and confinement in CMOS, the same fundamental index guiding principles can be used to obtain phononic waveguiding in conventional CMOS platforms by utilizing periodic FEOL/BEOL materials within the constraints of the Design Rules (DRs) set by the technology under consideration. Depending on availability of electromechanical transduction mechanisms in the FEOL and/or BEOL regions, the aforementioned grating can be created using transistor layers and source-drain-gate contacts or using BEOL transducer materials respectively. The resulting grating waveguide is a slow wave structure capable of supporting modes with acoustic velocities lower than the substrate and other surrounding regions. **Figure 2C** shows the schematic for a FEOL phononic waveguide implemented in a planar CMOS process with the distinct regions necessary for efficient waveguiding. In modern CMOS process nodes the BEOL dielectrics are typically low- k dielectrics which have higher viscoelastic loss as compared

to the high intrinsic Q-factor silicon substrate. Therefore, it is important to confine the mode as close to the substrate and as far away from the BEOL dielectrics as possible to achieve a high overall Q-factor. While the FEOL grating by itself, bounded by the substrate and the BEOL material stack, may be capable of sustaining a waveguide mode, this would be a sub-optimal implementation because of significant field penetration into the lossy BEOL materials. For further confinement in the z -direction, a BEOL Phononic Crystal (PnC) structure comprised of the available metal levels is utilized as shown in **Figure 2C**. In this section, each of these design aspects associated with CMOS grating waveguide resonators is discussed in further detail.

3.1 BEOL PnC Design

Phononic crystals are the acoustic analogues of photonic crystals (Kushwaha et al., 1993; Sigalas and Economou, 1993) composed of periodic arrangement of materials having different acoustic velocities. PnCs exhibit effective material properties that are not otherwise achievable using conventional materials (Khelif and



Adibi, 2015). One emergent macroscopic property from the periodic nature of PnCs is the existence of acoustic band-gaps (BGs), which are frequency ranges within which acoustic waves are forbidden to propagate. Acoustic wave manipulation in SAW and slab propagation scenarios such as in (Olsson and El-Kady, 2008) has been previously demonstrated to create a gamut of devices ranging from PnC waveguides and resonators to add-drop filters. PnCs having band-gaps centered on resonance frequencies have been employed to enhance the Q-factor of MEMS resonators by either being used as tethers for the released structure (Wang and Weinstein, 2011; Lin et al., 2014; Wang et al., 2015; Gokhale and Gorman, 2017; Rawat et al., 2017) or in the surrounding region to prevent acoustic energy leakage (Siddiqi and Lee, 2018).

PnCs for acoustic wave or modal confinement at RF and mm-Wave frequencies in CMOS can be realized using patterned BEOL metals embedded in dielectric materials (Bahr et al., 2014; Bahr et al., 2015; Anderson et al., 2021), used for electrical routing on chip. The primary goal of the BEOL PnC design is to maximize the phononic band-gap by optimizing the lateral metal width/spacing and *via* inclusion/exclusion limited by the waveguide lattice constant and the design rule checks (DRCs). The optimized PnC is then used to confine the mode in the FEOL grating and transduction layer by preventing acoustic propagation vertically up through the CMOS stack. Acoustic impedance contrast between the BEOL metal and dielectric materials specific

to the process is one of the primary factors that determines the band-gap width.

A higher impedance contrast is expected to lead to a higher band-gap width, hence CMOS processes such as planar IBM12RF and FinFET GF 14LPP with copper (Cu) metal and low-k dielectrics are capable of producing band-gap widths ranging from 1.07 to 3.8 GHz. On the other hand, low impedance contrast processes such as the IBM 130 nm and XFab 180 nm processes that make use of copper (Cu) or Tungsten (W) metals embedded in the Silicon-di-Oxide (SiO_2) dielectric result in significantly lower band-gaps ranging from 0.3 to 0.72 GHz (Bahr, 2016b). PnCs implemented in older process technologies that make use of Aluminum as the BEOL metal do not provide a usable bandgap. This is owing to the low impedance contrast between Aluminum and the BEOL dielectric material (primarily SiO_2 in these processes).

Figure 3A illustrates the implementation of a 2D PnC unit cell in the IBM12RF process BEOL for vertical acoustic confinement with the corresponding band structure. The band structure depicting the dispersion characteristics of the PnC are obtained using FEM Eigenfrequency simulations with Floquet Periodic Boundary Conditions (PBCs) by spanning the wave-vector \vec{k} along the edges of the Irreducible Brillouin Zone (IBZ) as shown **Figures 3A,B**. A complete band-gap of 3.03 GHz is obtained for the 2D PnC under consideration. **Figure 3B** illustrates the phononic bandstructure of a BEOL reflector plate having the same Cu thickness and unit cell dimensions

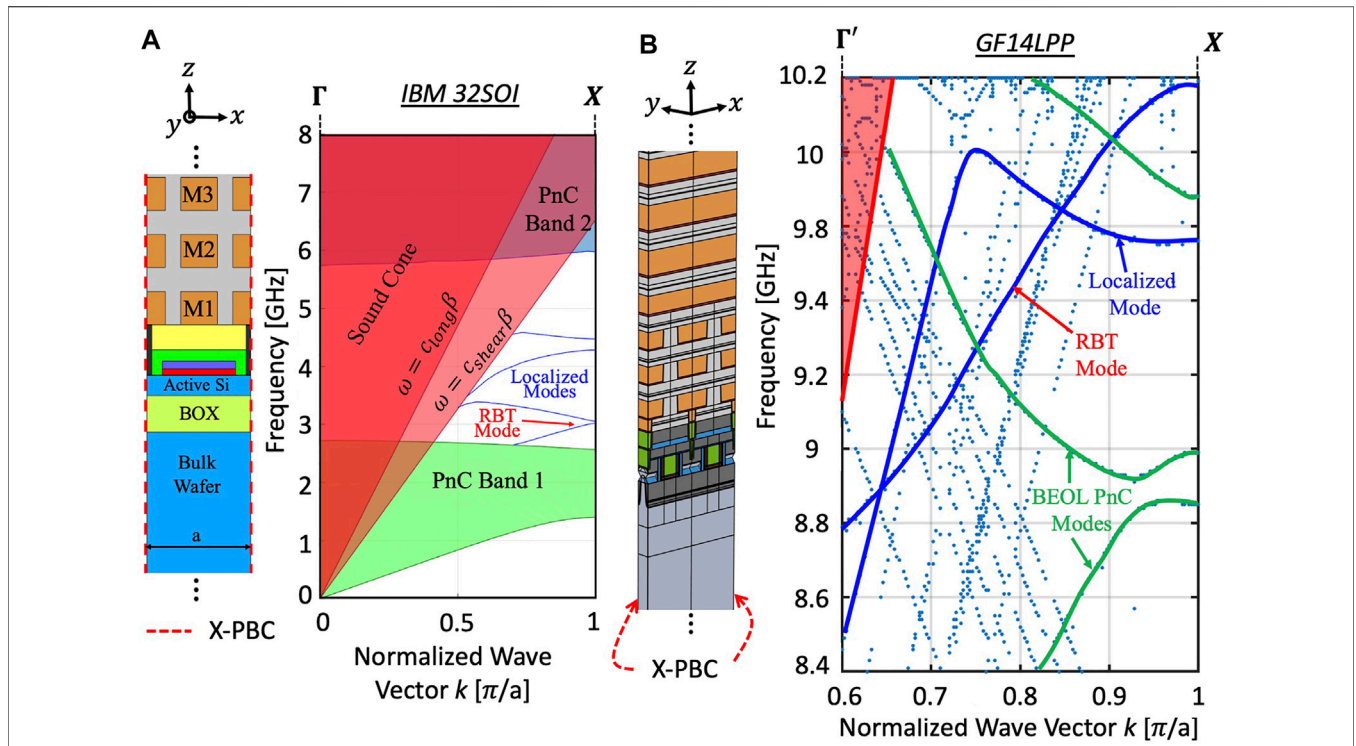


FIGURE 4 | (A) A single waveguide 2D unit cell with x-direction periodic boundary conditions corresponding to the IBM12RF process together with its bandstructure showing various modes that exist and the sound cones. This figure is a reprint of **Figure 3** in (Bahr and Weinstein, 2016) reprinted with the permission of the Transducer Research Foundation **(B)** A 3D waveguide unit cell for the fin-Resonant Body Transistor (fRBT) device implemented in the GF14LPP process and the corresponding bandstructure with different modes.

as the PnC unit cell in **Figure 3A**. Comparing the dispersion characteristics of the two types of cells, it can be seen that the reflector plate exhibits only a partial BG of 3.49 GHz along the X-M direction and not a complete BG like the PnC. This implies that the reflector plate, while capable of providing confinement for acoustic waves perfectly along the X-M direction, is not capable of blocking oblique leakage in the Γ -M direction like in the PnC. The reflector plate provides inferior overall confinement. However, in cases where DRC prohibits PnC dimensions corresponding to required BG characteristics, it is a valid option for device design. As an example in the case of a 32 GHz Resonant Fin Transistor design, PnC dimensions small enough for creating a BG around these frequencies are not allowed, thus multi-metal layer plate reflectors are employed (Bahr et al., 2018).

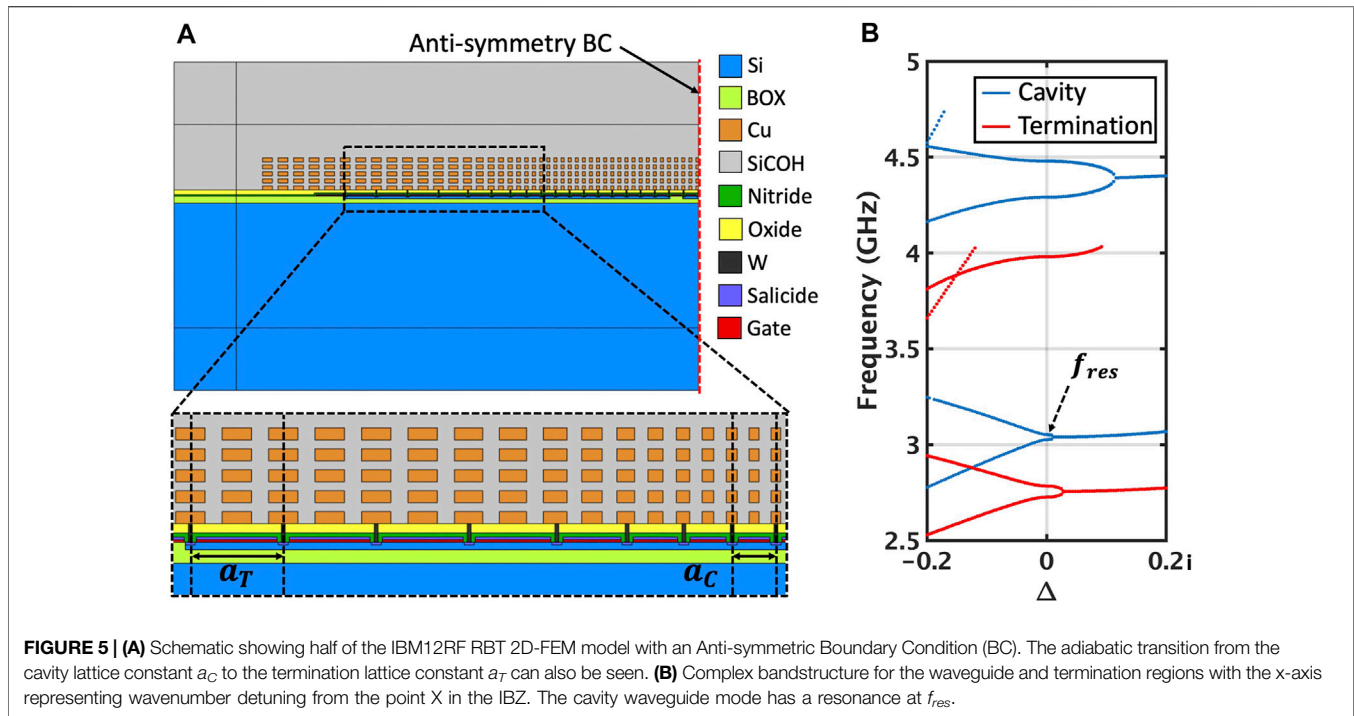
3.2 Waveguide Dispersion Engineering

As has been established, phononic waveguiding is achieved in CMOS FEOL layers through index guiding and vertical PnC confinement. When appropriately designed, the guided mode is confined in the FEOL region with maximum stress concentration around the channel region of transistors, where electromechanical transducers are located. Waveguide acoustic dispersion is critical in optimizing device performance. The same 2D FEM Eigenfrequency simulation procedure used in the case of the PnC dispersion characteristics is also used for waveguides.

Since the waveguide structure is periodic along the propagation x -direction only, single 2D and 3D array elements as shown in **Figure 4A** for IBM 32SOI RBT and (b) for GF14LPP RBT, respectively, are used to calculate the dispersion characteristics by varying the x -component of the wave-vector \vec{k} i.e. k_x along the edge of the IBZ.

From the obtained dispersion characteristics as shown in **Figure 4**, it can be seen that a multitude of modes, which are valid Eigenstate solutions for the structure, are obtained. Of these, localized waveguide modes lying below the longitudinal and shear wave sound cones of the substrate are of interest since these modes propagate in the FEOL region where they can be actuated and sensed effectively. BEOL PnC modes propagate only in the PnC region and are not capable of being interacted with electromechanically. For minimizing the acoustic leakage into the bulk substrate, the effective $|\vec{k}|$ distance between the point X in the IBZ and the edge of the soundcone at the same frequency is to be maximized. This ensures the lowest coupling of the targeted RBT mode to the bulk propagation states improving the mode index guiding and thereby raising the overall Q-factor.

The device designer has multiple avenues for augmenting the targeted mode by tuning the waveguide structural parameters within the confines of the DRCs to get the desired Q as well as effective electromechanical transduction. As can be inferred from the unit cells in **Figure 4**, a change in the transistor gate length changes the dispersion characteristics which can be used to set the



resonance frequency to the desired value as well as to design appropriate waveguide terminations (discussed later). To enhance stress concentration in the gate/channel region of the transistor, it is sometimes useful to add a gate contact along with the first level metal routing to the unit cell. For a given lattice constant, the width and spacing of the BEOL metal PnCs can be also be adjusted to maximize channel stress. Similarly, in the case of BEOL phononic waveguides comprising of FeCAP transducers (He et al., 2019; He et al., 2020), the lower limit of the spacing between the individual transducers as set by the DRCs governs the attainable lowest frequency. The available degrees of freedom for tuning the waveguide dispersion are the transducer length, addition/removal of vias and the BEOL PnC metal width, spacing and arrangement.

3.3 Lateral Acoustic Confinement

While index guiding and BEOL PnCs allow for vertical confinement in the z-direction, in order to create a resonator, terminations in the horizontal x- and y-directions are also required. The terminations on either side of the waveguide along the direction of propagation (x-direction) act as reflectors, trapping energy within the waveguide cavity where electromechanical transduction can occur. The efficiency with which the terminations reflect acoustic energy back into the cavity determines the overall Q-factor of the device considering radiative losses. The primary goal in designing appropriate terminations for the waveguide cavity is to provide adequate reflectivity while minimizing scattering at the cavity-termination boundary.

Initial waveguided RBT designs such as those demonstrated in (Bahr et al., 2015) relied on reflections due to abrupt cavity terminations on either side together with a Tungsten contact bulk

tie. While the acoustic impedance mismatch between the cavity and the termination regions does provide reflection, it also introduces significant amount of bulk scattering which is one of the factors limiting the overall measured Q-factor of the device to 260. A more efficient method for lateral confinement is to use the termination waveguides which have the same structure as the cavity waveguide but a different lattice constant as shown in **Figure 5A**. As can be seen in the complex dispersion relations in **Figure 5B**, the targeted RBT mode in the cavity region is not capable of coupling to any of the guided modes in the termination waveguide at the same frequency f_{res} because of the significant distance between them in the k - space. A large wavenumber detuning Δ is required for coupling between guided modes in the cavity and termination waveguides leading to confinement. While there may be low k - space overlap between the targeted mode and the BEOL PnC modes in the termination at the same frequency, the spatial separation and polarization difference between them prevents any coupling from taking place. The termination lattice constant is optimized for the maximum Q-factor associated with radiative losses. 2D and unit-cell based 3D finite element models are indispensable for overall device design but do not take into account finite cavity aperture along the y-direction. Dispersion engineering similar to that in laterally confined SAW devices (Inoue et al., 2007; Solal et al., 2010; Inoue et al., 2013) ensures that there is minimal lateral acoustic leakage out of the cavity and into the surrounding regions.

To further improve lateral confinement, smooth adiabatic transition from the cavity lattice constant to the termination lattice constant can be employed. According to the Adiabatic Theorem (Johnson et al., 2002; Bahr, 2016b), a sufficiently slow transition from the cavity to terminations can practically

eliminate any scattering at their interface. This technique has previously been adopted for photonic waveguides (Johnson et al., 2003; Üstün and Kurt, 2011; Oskooi et al., 2012) to couple light into slow light structures and for creating adiabatic bends. Other equivalent phononic demonstrations of adiabatic transitions can be seen in (Dehghannasiri et al., 2016; Shao et al., 2019).

3.4 Effective Modal Transduction

The transducers, whether in FEOL or BEOL, form a part of the cavity waveguide. Hence, effective electromechanical transduction is closely linked to the mode design, drive/sense configuration, constraints set by the DRCs and the transducer type. From a general drive transducer perspective, to maximize energy transfer to the device, the physical overlap between the transducer drive force and the modal displacement displacement field should be maximized. This can be quantified using the following equations (Rawat et al., 2022) for the equivalent displacement of a mode together with the resulting effective stiffness k_{eq} :

$$W_e = |F_e|u_{i,eq} = \frac{1}{A_{act}} \iint_{A_{act}} \vec{F}_e \cdot \vec{u}_i dA \quad (1)$$

$$k_{eq} = \frac{2E_{stored}}{|u_{i,eq}|^2} \quad (2)$$

where \vec{F}_e is the applied electrostatic force, $u_{i,eq}$ is the equivalent modal displacement, \vec{u}_i is the vector displacement field of the actuation surface having an area A_{act} , and E_{stored} is the stored energy. In a sub-optimal design, the drive force and the displacement field maxima are misaligned causing a reduction in the effective displacement, increase in the effective stiffness, and hence a reduction in the motional capacitance of the mechanical series equivalent circuit. The transduction efficiency (k_{eff}^2) which is given by the ratio of the motional capacitance to the static transducer capacitance, reduces. This implies that in a sub-optimal design, the majority of the incident electrical signal is reflected back with a small fraction of the overall energy making it to the device. This is also applicable for the sense transducer. This transducer design principle highlights an important trade-off in the overall device performance wherein the mode design for requirements for high-Q and high- k_{eff}^2 may be at odds. It may so happen that the designed mode maximises the overlap integral in Eq. 1 but in doing so the mode is concentrated in low-Q materials such as metals and intermetal dielectrics, which lowers the overall Q-factor. In the case of transistor sensing as implemented in the IBM12RF and GF14LPP devices, the primary goal is to design the mode such that the stress in the transistor channel can be maximized. Additionally, in order to ensure that the k_{eff}^2 is maximized, modes have to be designed such that the ratio of the transducer volume to the overall modal volume is as high as possible.

At the frequency corresponding to the mode of interest, it can be observed from the typical bandstructure of a waveguide unit cell (Figure 4A), that it is possible to excite not only the targeted mode but also modes that are either close to or within the sound cone. If the coupling between the drive force and the modes in the sound cone is significant, it would result in low Q

due to radiative losses through modes that can propagate freely in the substrate. The designed waveguide modes typically operate at point X in the IBZ which means that the acoustic fields in adjacent unit cells in the cavity are 180° out of phase as shown in Figure 6A. To minimize coupling to the sound cone and to maximize coupling to the targeted mode, fully differential drive and sense transduction is preferred in the cavity, corresponding to a single large spatial frequency component at point X in the k - space IBZ. A complete mathematical treatment for the same can be found in (Bahr, 2016b). Fully differential drive and sense is also useful from an applications perspective since it eliminates any common-mode noise. It may not always be possible to achieve fully differential drive and sense, in the case of the Resonant Fin Transistor (RFT) devices it is not possible to differentially contact each transistor fin owing to DRC restrictions. In such cases a compromise is reached by driving three adjacent fins and skipping four fins in between as shown in Figure 6B. This configuration is also capable of driving the differential mode albeit with a lower coupling since one of the three fins in the transducer finger has an opposite acoustic field polarity to the other two resulting in overlap cancellation.

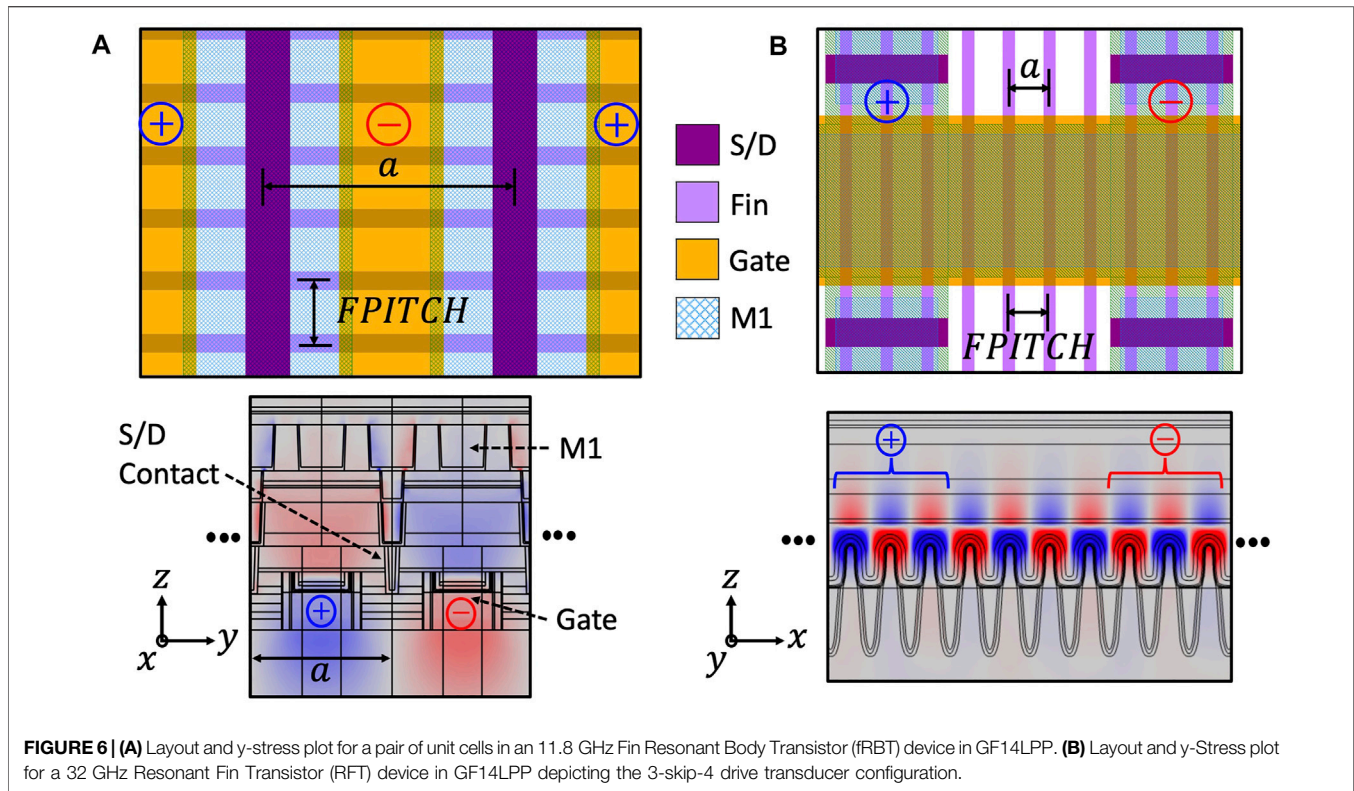
4 ELECTROMECHANICAL CONVERSION

For electromechanical drive and sensing, there are many CMOS-integrable transduction mechanisms (Huber et al., 1997; Yang and Xu, 2017) that may be used including the shape memory effect (Hunter et al., 1991), phase transition materials (Shi et al., 2019; Huang et al., 2021), and electrothermal (Gilgunn et al., 2008; Koh et al., 2011; Zope et al., 2020). Shape memory alloys and phase change actuators promise large work densities for demanding microrobotics applications, but have not yet been integrated in any commercial CMOS technology. These technologies are also limited to relatively low duty cycles (kHz to low MHz) that make them unsuitable for high frequency transduction.

Electrothermal actuators are notable in that they are easily realizable in commercial MEMS processes (Abbasalipour et al., 2018) and offer moderate work densities (Zope et al., 2020). Furthermore, they are predicted to scale well into the GHz regime (Rahafrooz and Pourkamali, 2011; Ramezany and Pourkamali, 2018) as thermal time constants decrease with decreasing size. Most commonly used, however, is direct energy-conserving electromechanical conversion using capacitive and piezoelectric transducers.

4.1 Capacitive Transduction

Air gap capacitive transduction has been successfully utilized in commercial devices for many years (Partridge and Tabatabaei, 2009). Such devices are typically integrated either at the wafer packaging level or through custom post-processing (Fedder et al., 2008; Lopez et al., 2009; Chen et al., 2011; Lapisa et al., 2011). Since the electromechanical coupling coefficient in air gap transducers increases as gap size shrinks, significant effort has gone into innovative processing techniques



for achieving high aspect ratio structures (Ayazi, 2002; Ozgurluk et al., 2020). As target frequencies scale into the mmWave spectrum and required physical dimensions approach 10s of nm, a more practical solution is to utilize the dielectric layers available in the standard CMOS stack for internal dielectric transduction, where the driving dielectric is incorporated into the resonant structure (Weinstein and Bhave, 2009). Such an approach avoids the processing challenges of a high aspect ratio air gap release step, eliminates concerns over stiction that arise as air transducer gap sizes shrink, and provides a motional impedance that shrinks with increasing frequency and with decreasing dielectric thickness. At high enough frequencies (700 MHz–8 GHz in silicon, crystallographic orientation dependent), the acoustic wavelength scales below the phonon mean free path length of the material (the Landau-Rumer regime), leading to $f \times Q$ products that scale with increasing frequency (Braginsky et al., 1986; Tabrizian et al., 2009). Beyond the standard dielectrics available in CMOS, it is also possible to utilize a reverse biased diode's depletion capacitance in place of a standard dielectric film (Hwang and Bhave, 2011). This approach combines the scaling benefits of internal dielectric transduction with the potential to utilize a high-Q single crystal silicon resonator structure and was further integrated with JFET sensing in (Hwang et al., 2011). The main challenge of depletion-layer actuation comes from designing a resonant structure of interest around the available junctions in each technology. In SOI processes this approach can be combined with a release step to remove

underlying oxide, obviating the need for a waveguided mode to prevent energy leakage to the underlying layers. Select capacitive resonators operating at low voltage in very high frequency (VHF) and above are highlighted in **Table 2**.

4.2 Piezoelectric and Ferroelectric Transduction

Compared to capacitively-transduced resonators, piezoelectric transducers are highly desired for their high electromechanical coupling coefficient which enable large fractional bandwidths required for 5G and beyond (Yang et al., 2020). Research efforts in this area include $\text{Al}_x\text{Sc}_{1-x}\text{N}$ (Fichtner et al., 2019), LiNbO_3 (Hackett et al., 2021), $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ [PZT] (He et al., 2020), HfZrO_2 [HZO] (Hakim et al., 2021) and doped HfO_2 thin films (Schroeder et al., 2014; Anderson et al., 2018). BAW resonators based on AlN (Ruby et al., 2001a) and LiNbO_3 SAW devices in standalone packaged chips have been available for several years. Work on the commercial integration of LiNbO_3 with silicon is ongoing (Lee et al., 2003) and $\text{Al}_x\text{Sc}_{1-x}\text{N}$ has been demonstrated co-packaged with CMOS (Shih et al., 2019; Liu et al., 2020). PZT, on the other hand, is commercially available in the CMOS BEOL in the Texas Instruments 130 nm FeRAM process. PZT and low leakage $\text{Al}_x\text{Sc}_{1-x}\text{N}$ films have typical thicknesses of 100+ nm (Fichtner et al., 2020), with recent $\text{Al}_x\text{Sc}_{1-x}\text{N}$ films demonstrated with some leakage down to 25 nm (Rassay et al., 2021). While chemical solution deposited HfO_2 and HZO films have been demonstrated as thick as $1 \mu\text{m}$ (Schenk et al., 2020), other deposition techniques generally range from 50 nm (Quan et al., 2020; Tharpe et al., 2021a) down to sub-10 nm thicknesses (Wei

TABLE 2 | Overview of several approaches to scaling capacitive transduction via shrinking air gap thickness and utilization of depletion capacitance actuation.

Transduction mechanism	Gap size (nm)	Resonance frequency (MHz)	Q-factor	V _{dcl} (V)	Ref
HARPSS Air Gap	65	81.2	40,100	10	Pourkamali et al. (2007)
ALD Gap	10	223	67,920	5	Cheng and Bhawe, (2010)
ALD Gap	8	199.8	12,298	0.6	Ozgurluk et al. (2020)
Diode	n/a	3,721	18,000	5	Hwang and Bhawe, (2011)
Diode/JFET	n/a	1,610	25,900	5	Hwang et al. (2011)

For MOSFET sensed resonators, see **Table 1**.

et al., 2018), opening the door for piezoelectric integration into the FEOL transistor gate oxides (Trentzsch et al., 2016).

In addition to their piezoelectric properties, all of these films with the exception of AlN also exhibit ferroelectricity - the formation of a bistable polarization state in response to applied electric field. Perovskite-based ferroelectric RAM (FeRAM) has been a commercial product for many years and is prized for long retention times and radiation hardness (Arimoto and Ishiwara, 2004; Gerardin and Paccagnella, 2010), but has been limited in application scope due to large (100+ nm) ferroelectric film thicknesses required to achieve a usable memory window. With the advent of highly scaled ferroelectric films in the last 11 years, ferroelectric polarization-based memory is now a leading contender for next-generation CMOS memory (Trentzsch et al., 2016). The polarization of these ferroelectric films can be represented via the Landau-Khalatnikov model as a double-well free energy landscape with respect to dielectric polarization charge. As external electric field is applied to the ferroelectric, the energy landscape tilts until one well vanishes (at the coercive field, E_c) and the state of the ferroelectric domain switches, as shown in **Figure 7A**. When field is removed, the ferroelectric film will settle into a non-zero remnant polarization, P_r (Rabe et al., 2007).

Much like flash memory, where trapped charge on a floating gate leads to a threshold voltage shift in the associated transistor, ferroelectric remnant polarization can also be used to induce a threshold voltage shift when integrated as a gate dielectric in transistors. Unlike flash, however, polarization charge comes from the state of the crystal lattice, leading to potentially enhanced endurance (Trentzsch et al., 2016). One concern in metal-ferroelectric-semiconductor devices is the presence of a depolarization field across the ferroelectric when bias is removed, reducing retention time. This is due to required charge neutrality between the ferroelectric film and any dielectric buffer layer that may exist at the ferroelectric-semiconductor interface, and should be minimized by maximizing the ratio of the buffer layer to ferroelectric film capacitance (Arimoto and Ishiwara, 2004). Ferroelectric switching voltage for these memory devices (and for programmable ferroelectric transducers) is set by the coercive voltage - given by the product of coercive field and ferroelectric film thickness. In metal-ferroelectric-insulator-semiconductor (MFIS) structures, the write voltage required may be much higher due to voltage drop across the buffer layer, as well as asymmetric due to non-zero flat band voltage and semiconductor surface potential. This is described by

$$V_{\text{applied}} = V_{\text{ferro}} + V_{\text{dielec}} + \Psi_s + V_{fb}, \quad (3)$$

where V_{applied} is the total voltage applied to the stack, V_{ferro} is the voltage in the ferroelectric layer that contributes to switching and transduction, V_{dielec} is the voltage drop across a dielectric buffer layer, Ψ_s is the semiconductor surface potential, and V_{fb} is the flat band voltage of the MFIS stack (Anderson et al., 2018). For example, a 10 nm ferroelectric HfO₂ thin film with a 1 nm interfacial SiO₂ may result in over 1/3 of the applied voltage dropping across the dielectric due to the large difference in permittivity between the two films. Of an applied voltage then, only a fraction may go to switching the ferroelectric film, lowering attainable P_r vs. an equivalent metal-ferroelectric-metal stack in the same V_{DD} . This must be taken into account along with E_c if designing an FEOL MFIS transducer to determine the maximum thickness of ferroelectric material usable for a given process supply voltage.

In polycrystalline thin films, there exist several domains with independent states and a distribution of coercive fields, leading to the potential for intermediate states of remnant polarization. With domains all aligned in the same direction, these films behave similarly to standard piezoelectric films. If partially switched, however, the piezoelectric response of opposing domains will be out of phase and will cancel each other out, leading to a lower effective coupling coefficient (He et al., 2020). This phenomenon can be leveraged for programmable transduction in applications such as voltage controlled oscillators as well as adaptive filters. As these devices are scaled down in area the total number of domains decrease and analog-like ferroelectric switching gives way to discrete jumps in polarization charge as individual domains switch, which may limit tuning in some analog applications (Mulaosmanovic et al., 2017).

The coercive field required to switch thin film ferroelectric domains is not constant with frequency, but rather increases as pulse width decreases, with switching commonly limited by domain propagation in thicker films (Fichtner et al., 2020) and domain nucleation limited switching demonstrated in 10 nm Si:HfO₂ films (Mulaosmanovic et al., 2017). This property, while limiting the speed at which radios utilizing ferroelectrics can be reconfigured, can also be exploited to provide fine tuning of resonators, with sensitivity of domains to a specific programming voltage determined by programming pulse width (Dabas et al., 2022).

The ferroelectric properties of these films are also temperature sensitive. As seen in **Figure 7B**, the energy barrier between states

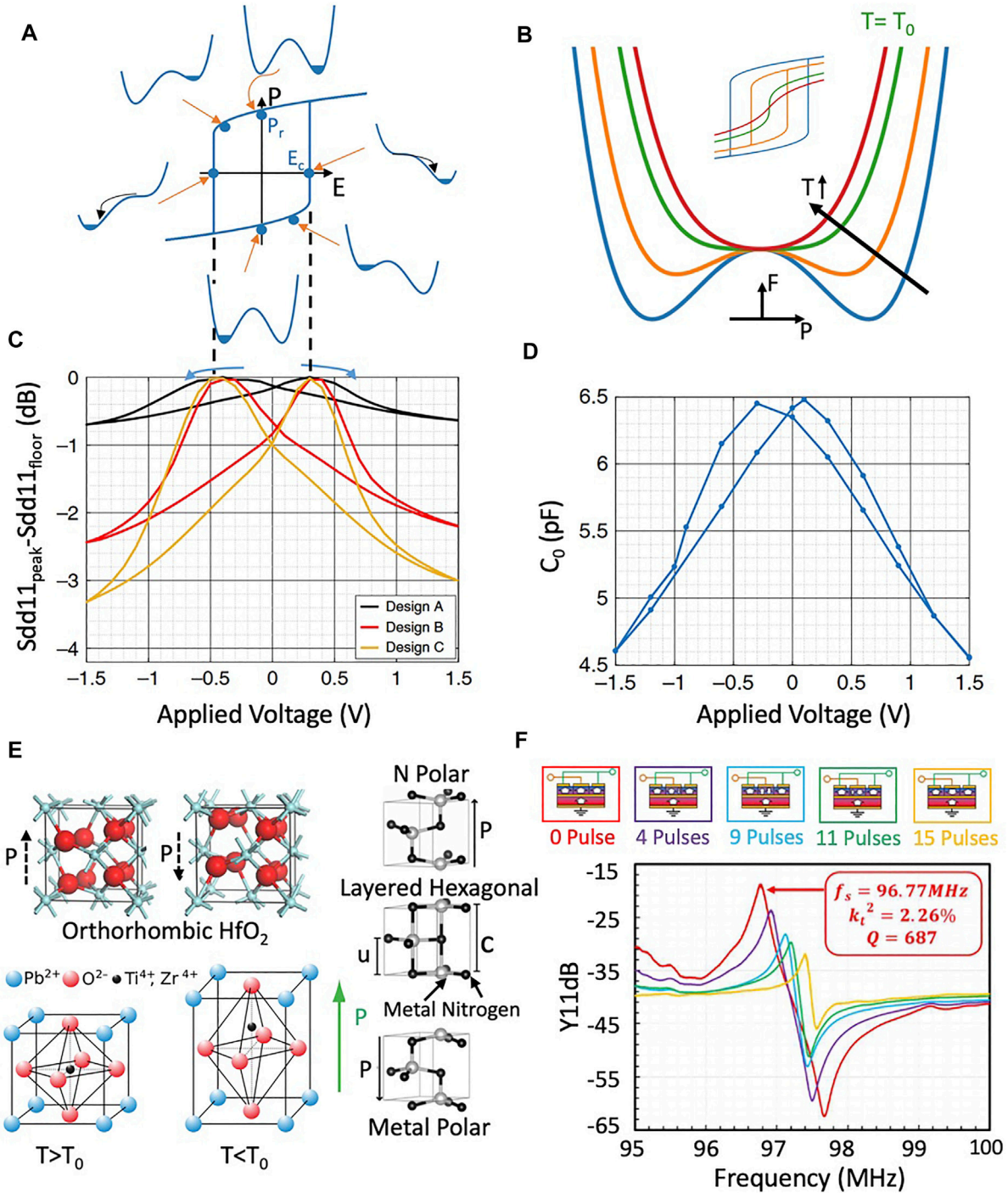


FIGURE 7 | (A) Ferroelectric films exhibit two stable energy states at nonzero polarization, modeled via Landau theory (Rabe et al., 2007). When applied field tilts the energy landscape of the ferroelectric domain such that the occupied well disappears, the domain switches into the other polarization state. **(B)** As temperature increases, the depth of the wells in the free energy profile decrease (decreasing coercive field) until they disappear altogether at the Curie temperature (shown in green). Above this temperature (red curve), hysteresis disappears and the stable energy minimum occurs at zero polarization, as shown by the inset. The differential curvature of this profile, proportional to the inverse of capacitance, approaches zero at the Curie temperature, leading to a large increase in effective dielectric constant near zero field. **(C)** The programmability of ferroelectric hysteresis for tunable transduction has been experimentally demonstrated in CMOS (He et al., 2019) with parallel resonance in Sdd11 trending to zero at the coercive voltage as shown in (A) Designs A-C all share a unit cell design, but highlight some of the techniques that can be used to reduce scattering and boost quality factor in unreleased resonators. Designs B and C employing lateral terminating blocks as discussed in Section 3.3 to extend the cavity periodicity beyond the transduced region, while C furthermore replaces square array vias in the out of plane direction with a single rectangular via, reducing scattering. **(D)** These devices also demonstrated a change in electrical capacitance as a function of bias due to the non-quadratic energy landscape associated with ferroelectrics. **(E)** (Continued)

FIGURE 7 | Unit cells, clockwise from top left, of ferroelectric materials PZT, AlScN, and HfO₂ show bi-stable non-centrosymmetric behaviour indicative of ferroelectric materials (Rabe et al., 2007; Pinin, 2010; Boescke et al., 2011; Fichtner et al., 2019). **(F)** Coercive field is not a set value but is a function of pulse width and voltage level, with probabilistic switching of domain. This has been exploited in (Dabas et al., 2022) to explore partial switching of AlScN at lower voltages for applications in temperature compensation. HfO₂ structure in **(E)** reproduced from Boescke et al., 2011 with permission of AIP Publishing. Parts **(C–E)** excepting PZT unit cell copyright IEEE, reprinted from (He et al., 2019; Fichtner et al., 2020, and Dabas et al., 2022) with permission.

TABLE 3 | Potential value calculated given a stiffness of 320 GPa (Tharpe et al., 2021b), while permittivity and piezoelectric coefficients are taken from (Kirbach et al., 2018).

	Thickness (nm)	k_{eff}^2 (%)	P_r ($\mu\text{C}/\text{cm}^2$)	E_c (MV/cm)	T_0 (K)	Ref
LiNbO ₃	800+	31	71	0.04	1,483	(Kim et al., 2002; Lee et al., 2003; Rabe et al., 2007; Hussein et al., 2022)
PbZr _x Ti _{1-x} O ₃	100+	0.047–7.3	31	0.05–0.25	523–770	(Hooker, 1998; Zinck et al., 2004; Bouzid et al., 2005; He et al., 2020)
Al _x Sc _{1-x} N	25–1,000	2.8	100	2–5	870	(Fichtner et al., 2019; Liu et al., 2020; Ledesma et al., 2021; Rassay et al., 2021; Wang et al., 2022)
HfO ₂	5–50	4.7–30.7 ^a	30	1–2	809	(Kirbach et al., 2018; Wei et al., 2018; Gastaldi et al., 2021; Hakim et al., 2021)
[Hf/Zr]O ₂ [CSD]	45–1,000	6.6	10–20	1–1.5	—	(Starschich et al., 2014; Starschich et al., 2017; Schenk et al., 2020)

HfO₂ rows include HZO and doped HfO₂ films. Experimentally demonstrated k_{eff}^2 from Si-integrated devices. For PZT, the lower value indicates reported k_{eff}^2 from unreleased BEOL integrated resonators in the TI process (He et al., 2020) while the higher number is a released FBAR (Zinck et al., 2004). This situation is reversed for emerging HfO₂ films, where film stress (through dopants, electrodes, deposition technique, etc.) plays a large role in ferroelectric stabilization (and hence, k_{eff}^2) (Boescke et al., 2011; Schroeder et al., 2014; Hoffmann et al., 2015; Tharpe et al., 2021b). Properties also vary with material composition and/or doping percentage and have been shown to decrease on film release, hence calculated potential k_{eff}^2 based on some reported unreleased film parameters is also shown. 1 MV/cm = 1 V per 10 nm of film, thus HfO₂ and Al_xSc_{1-x}N are desirable as thin films for low voltage programmable operation, whereas LiNbO₃ and PZT films are desirable in 0.1–1 μm thicknesses to achieve a usable polarization window. Chemical solution deposited HfO₂ films are unique in the large thicknesses achievable while maintaining ferroelectric behaviour and as such are highlighted separate from other deposition techniques.

^aPotential value calculated given a stiffness of 325 GPa (Tharpe et al., 2021b), while permittivity and piezoelectric coefficients are taken from (Kirbach et al., 2018).

decreases with increasing temperature until a critical point (the Curie temperature) at which the stable polarization states no longer exist (Rabe et al., 2007). These and other typical properties of leading ferroelectric films are given in **Table 3**, with the polarizable unit cells of PZT, Al_xSc_{1-x}N, and HfO₂ depicted in **Figures 7C–E**. While the Curie temperature is well above standard operating temperatures for CMOS devices, the changes in ferroelectric properties may be important for precision frequency or timing applications.

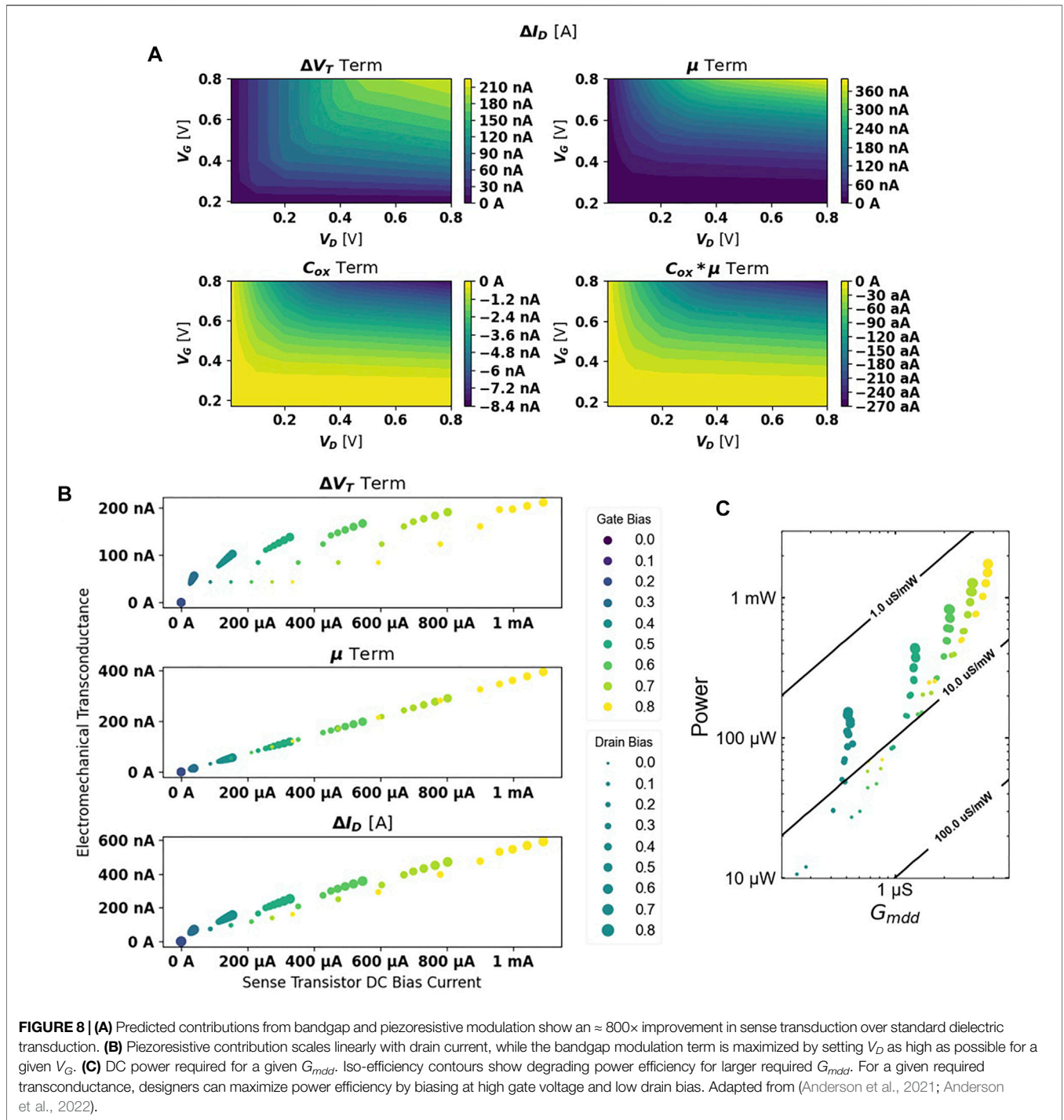
In hafnium oxide films, ferroelectricity emerges from the stabilization of a non-centrosymmetric orthorhombic phase (Boescke et al., 2011) through a combination of dopant species (Schroeder et al., 2014; Anderson et al., 2018), dopant distribution (Lomenzo et al., 2014), and electrode composition (Hoffmann et al., 2015) altering grain formation (Lederer et al., 2020) and providing stabilizing stress in the film, with even pure HfO₂ films showing ferroelectric behavior under 10 nm thicknesses (Polakowski and Müller, 2015). The impact of metalization before or after anneal of the ferroelectric properties of resulting HfO₂ ferroelectrics has been demonstrated (Mueller et al., 2012), as has the relaxation of stress due to HZO film release, decreasing orthorhombic phase and hence ferroelectricity (Tharpe et al., 2021b) - a property of particular concern for released MEMS applications. An additional complicating factor is the change in ferroelectric and piezoelectric properties with cycling (Mart et al., 2020; Kirbach et al., 2021) as individual grains rotate to align with applied field (Lederer et al., 2019). Experimentally reported $d_{33,f}$ values for HfO₂ ferroelectric films have reached 20 pm/V (Kirbach et al., 2018; Schenk et al., 2020), with even higher values predicted for doped ZrO₂ films (Falkowski and Kersch, 2020). Being measured from a thin film structure, this value is

expected to differ from bulk by a geometry dependent factor (Guo et al., 2013).

The coercive field of Al_xSc_{1-x}N films drops as Sc doping percentage increases, making the ferroelectric properties easier to utilize (Fichtner et al., 2020). This comes at the cost of decreasing P_r , however, so optimal material composition may change based on design requirements (Liu et al., 2020; Park et al., 2020). Additionally, the field at which domains switch in Al_xSc_{1-x}N films is on the order of a few MV/cm (Fichtner et al., 2020), requiring high voltages to switch at today's grown thicknesses. HfO₂ and PZT ferroelectrics, on the other hand, can be easily switched with voltages available in standard CMOS technologies.

4.3 Active Semiconductor Sensing

At mmWave frequencies, on-chip parasitics must be considered as part of integrated circuit design. Particularly in unreleased resonators, feedthrough capacitance can lead to poor stop-band rejection (Anderson et al., 2021) which must be overcome. One method to do so in FEOL-integrated resonators is to utilize available semiconductor devices to provide amplification in the mechanical to electrical conversion through bandstructure interactions. Semiconductor electron devices such as field effect transistors, junctionless nanowire transistors, and PN diodes are sensitive to strain and therefore able to detect acoustic vibrations (Weinstein and Bhave, 2010a; Hwang and Bhave, 2011; Bartsch et al., 2014). These active sense mechanisms offer opportunities to isolate and amplify the mechanical signal relative to electrical feed-through, providing enhanced sensitivity most critical in the GHz regime of operation. In addition, sense transistor biasing can also allow for real-time performance or power consumption tuning. When not in use, the sense circuitry



can be turned off altogether, whereas when in operation it can be operated at a maximum gate bias and the drain bias selected either in the linear regime for maximum efficiency or in the saturation regime for maximum performance (Anderson et al., 2021).

While atomistic simulation tools such as VASP (VASP, 2022), Quantum ATK (QuantumATK, 2022), and Victory Atomistic (Victory Atomistic, 2022) can be used to calculate

strained semiconductor band structure, a combination of empirical equations can also be used to account for the bandgap and mobility modulation in active sensors such as FETs, BJTs, and PN diodes. To a first order, the bandgap can be modeled to be linearly dependent on strain (Bardeen and Shockley, 1950). This modulation of the bandgap will result in a change in intrinsic carrier concentration and, hence, a change in the onset of strong inversion and a

shift in the threshold voltage of a transistor (Anderson et al., 2021).

Mobility modulation due to the carrier transfer effect and changes in effective mass can be captured with transverse and longitudinal piezoresistive coefficients (π) as

$$\mu(\sigma) = \frac{\mu_0}{1 + \pi_L \sigma_L + \pi_T \sigma_T} \quad (4)$$

and can be used in either active (Marathe et al., 2014; Anderson et al., 2018) or passive (Rahafrooz and Pourkamali, 2011; Abbasalipour et al., 2018; Ramezany and Pourkamali, 2018; Zope et al., 2020) sensing schemes. These coefficients change depending on crystallographic orientation and have been studied extensively in silicon (Kanda, 1991). While it is prudent to use average or effective stress/strain values for hand calculations with these equations, these effects can also be modeled as position-dependent and solved *via* TCAD if a detailed mode shape is known from finite element analysis (Li et al., 2012).

In FET transducers, these changes in semiconductor band structure are measured by a change in drain current. By observing the long channel square law model (Tsividis and McAndrew, 2010) it can be shown to the first order that the change in drain current due to dielectric transduction, the piezoresistive effect, and bandgap modulation can be written as

$$\Delta I_D = I_{D0} * (A_\mu + A_{C_{ox}} + A_\mu A_{C_{ox}}) - \Delta V_T * f\{\mu, C_{ox}, V_{DS}\} \quad (5)$$

for the linear regime and

$$\Delta I_D = I_{D0} * (A_\mu + A_{C_{ox}} + A_\mu A_{C_{ox}}) - \Delta V_T * f\{\mu, C_{ox}, V_{GS}, V_{DS}\} \quad (6)$$

in saturation, where A_μ , $A_{C_{ox}}$ are constants for a given stress and f represents a function multiplying ΔV_T (Anderson et al., 2021). As the contribution from dielectric transduction is relatively small compared to the piezoresistive modulation, it can be understood from these expressions that the transduced change in transistor drain current will have a piezoresistive component directly proportional to DC bias current, as well as a term that is a function of both the piezoresistive effect and bandgap/threshold voltage modulation. The impact of each of these components on transduction can be seen in **Figures 8A,B**. When implementing active semiconductor sensing in a new material or technology, care should be taken to verify that bandgap and effective mass modulation will not cancel each other or performance will be degraded.

In short channel devices, there are a number of effects that alter drain current including velocity saturation, vertical field degradation, drain induced barrier lowering, channel length modulation, gate-induced drain leakage, and quantum mechanical effects, among others (Colinge, 2008). Many of these effects are important since they reduce drain bias current and/or carrier mobility, lowering the transduced signal. Velocity saturation is notable in the fact that both optical emission and phonon emission - the two main mobility loss mechanisms as lateral field increases - are related to effective mass (Sze and Ng, 2006). Therefore, saturation

velocity V_{sat} is itself modulated with strain, with the relation modeled in (Lochtefeld and Antoniadis, 2001) as:

$$\frac{\Delta v_{sat}}{v_{sat0}} = \alpha \frac{\Delta \mu}{\mu_0} \quad (7)$$

with an experimentally measured α around 0.5.

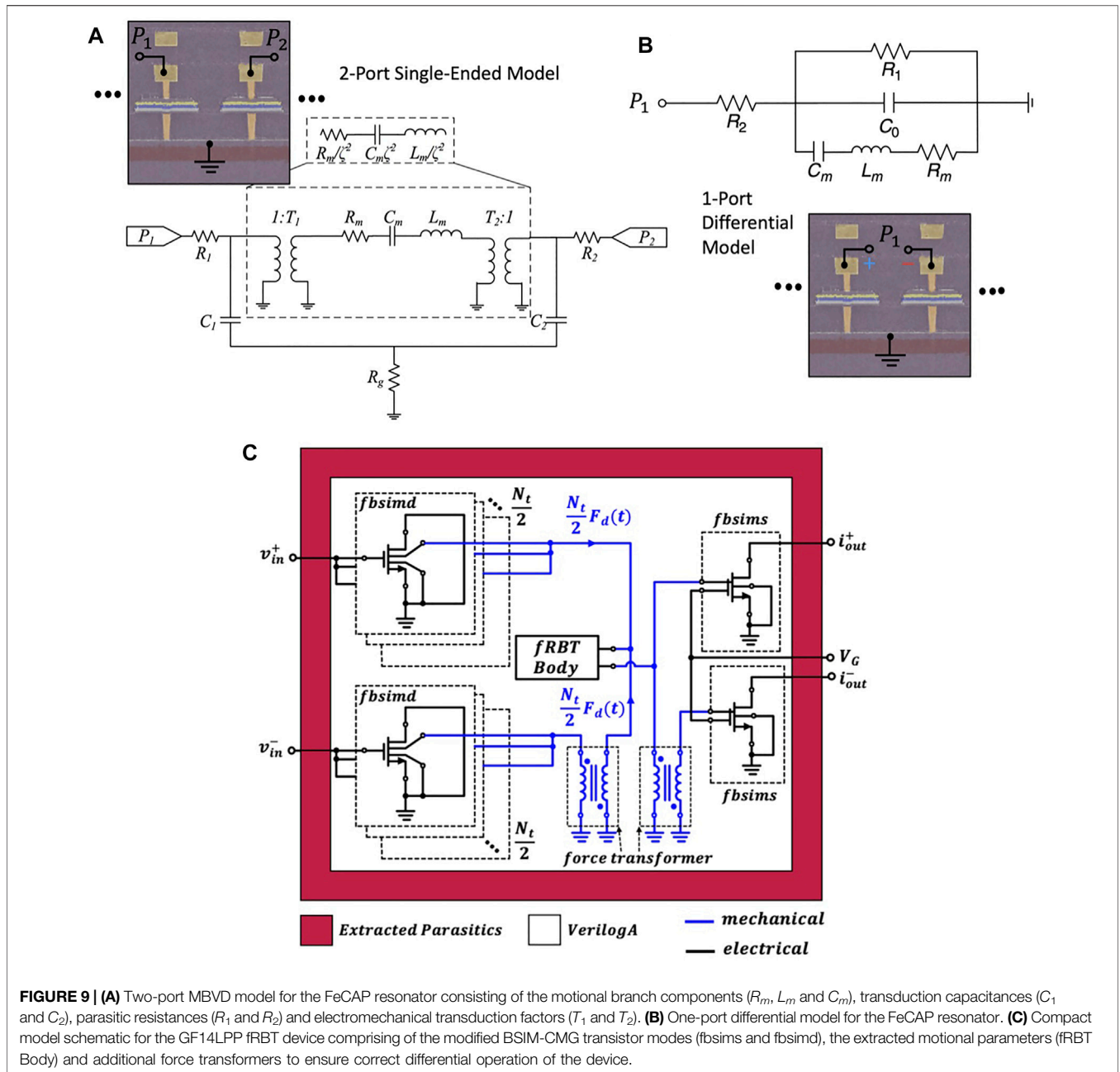
The largest challenge with unreleased CMOS-integrated active resonators demonstrated to date stems from relatively low mechanical transconductance (μS). 14 nm fRBT devices, highlighted in **Figure 8C**, require significant sense transistor current draw to achieve maximum g_{mdd} . This metric can be improved further through more efficient transduction using FEOL ferroelectric films as well as refinements to acoustic confinement in the cavity to enhance Q.

While the square law model is overly-simplified for today's commercial devices, a similar approach can be taken to implement these effects in more complex surface potential multigate models such as those utilized for finFETs (Colinge, 2008).

5 COMPACT MODELING

Prior to deploying monolithically-integrated CMOS-MEMS resonators in applications such as oscillators and filters, system-level simulations are required for design and performance tuning. Various tools such as Finite Element Analysis (FEA) for capturing the electromechanical behaviour, Electromagnetic/circuit extraction and TCAD for semiconductor physics are required to analyze and design the device itself but cannot be used collectively with modern circuit simulation methodologies. Therefore, low computational effort based accurate compact models that capture the device behavior, are validated against measured data and are capable of being used in all circuit simulation scenarios are required for monolithic CMOS-MEMS devices.

Typically, a modified Butterworth-van-Dyke (MBVD) model for capacitive and piezoelectric MEMS devices (Ruby et al., 2001b; Zuo et al., 2008; Lu et al., 2019) is obtained through extraction from RF measurement data. A typical two-port MBVD model primarily consists of a motional branch corresponding to the effective mass, stiffness and damping of the relevant resonance mode, transducer capacitance and a capacitive feedthrough branch in parallel with the motional branch. In the case of BEOL released CMOS-MEMS devices such as the one in (Chen et al., 2011), the conventional MBVD model is sufficient for system design. Other variants of such devices, as that in (Zope et al., 2020) employ thermal piezoresistive transduction which require changes to the MBVD model to reflect the appropriate transduction mechanisms. Models based on extracted data are capable of accurately capturing the device performance but need to be updated when design parameters are changed. Physics based compact models on the other hand are capable of predicting changes in device characteristics with a change in design. As discussed briefly in the previous section, monolithic capacitively-driven CMOS-MEMS devices have a very low k_{eff}^2 . The motional current is



completely buried under feedthrough in the intrinsic MOSCAP transducers making direct parameter extraction immensely challenging. Moreover, in systems and scenarios exhibiting large signal excursions, the small signal model is not expected to be accurate owing to the highly non-linear nature of the transduction mechanisms. Large-signal compact models have previously been developed for both released (Bahr et al., 2016b) and unreleased (Bahr et al., 2016c) RBT devices. Although these models are large signal in nature, they rely on the analytic formulations of the resonator mode shape and do not accurately capture the device parasitics. Integrated CMOS-MEMS devices almost always exhibit complex mode shapes

which are not possible to describe analytically. Electrical feedthrough between the device terminals owing to parasitics significantly influence the device performance making accurate extraction and parasitics model integration with the device model of significant importance. Since the device characteristics also vary with temperature, models are also required to be thermally-aware.

In the comprehensive large signal fRBT compact model (Figure 9C) described in (Rawat et al., 2022), an Eigenfrequency based extraction methodology is used together with accurate layout parasitic extraction and modifications of the BSIM-CMG finFET model (Duarte et al., 2015). This enables a

general modeling methodology for CMOS RBTs exhibiting complex mode shapes and physical interactions between electrical, mechanical and thermal domains. In the employed modal extraction methodology, an equivalence is established between the multi-degree-of-freedom (DoF) targeted resonant mode and a single DoF mass-spring-damper system using a 3D FEM Eigenfrequency simulation model. Modified BSIM-CMG models compatible with the GF14LPP process PDK are used for both the actuating MOSCAPs as well as the sense transistors to incorporate electromechanical conversion. The modified sense transistor model takes into account changes in transistor characteristics such as mobility, threshold voltage and saturation velocity due to stress in the resonant cavity. The full model for the device is fully integrated within the GF14LPP PDK enabling ease of system design and simulation. This measurement validated compact model for the fRBT device has also been shown to be applicable in simulation scenarios such as Periodic Steady State (PSS), Periodic AC (PAC) *etc.* In the case of BEOL-integrated FeCAP resonators, a version of the MBVD model as depicted in **Figure 9A** (He et al., 2019) is employed. In these devices, it is possible to bias the alternating transducers with distinct polarizations. Hence the electromechanical transformation ratios T_1 and T_2 for the two ports of the device can be distinct. Moreover, the bottom plate of the ferroelectric capacitors are all connected to a grounded poly-gate layer whose resistance R_g is incorporated into the model alongside other parasitic series interconnect resistances R_1 and R_2 . The parameter extraction is carried out by fitting the model response to the measured S_{21} of the device. In the case where the FeCAP resonators are to be operated differentially, a conventional MBVD model fitted to measured one-port differential S_{dd11} can be employed (He et al., 2020) as shown in **Figure 9B**.

6 SYSTEM DESIGN AND APPLICATIONS

The foremost applications of monolithic CMOS-MEMS resonant devices are in RF oscillator and filter designs across different frequency bands of operation. The primary consideration in the design of filters is achieving a large bandwidth of operation while having a low insertion loss in the passband. CMOS-MEMS resonant devices that exhibit a low k_{eff}^2 (capacitively transduced) are unsuitable for this particular application. Devices having CMOS-integrated ferroelectric materials would be the ideal candidates for filter design because of the significantly higher k_{eff}^2 values (**Table 3**). Filter design may be undertaken completely in the acoustic domain (Johnson, 1997; Bannon et al., 2000; Weinstein et al., 2007) or by electrically coupling multiple devices (similar to the designs in (Ruby et al., 2001a; Ruby et al., 2004; Piazza et al., 2007)). Since waveguiding in both the FEOL and BEOL regions of the CMOS stack has been successfully demonstrated, different coupled phononic cavity topologies may be used as depicted in (Olsson and El-Kady, 2008) to create add/drop filters. Because of the tunable nature of ferroelectric transduction, as demonstrated in (He et al., 2019; He et al., 2020), the resulting filters can be re-configurable in nature which is not feasible in conventional FBAR and SAW based

designs. A possible limitation of filters created using ferroelectrically transduced CMOS-MEMS devices is the nonlinear nature of ferroelectric transduction under the application of large signal swings which limits the power handling of these devices, thereby limiting the achievable Input Third Order Intercept Point (IIP3).

Availability of integrated ferroelectric transducers also enables the development of acoustic transducers/sensors for a wide variety of applications. High-overtone bulk acoustic resonance (HBAR) modes have been observed in measurement beyond the waveguided resonance frequency of the CMOS-MEMS FeCAP resonator (He et al., 2018; He et al., 2019; He et al., 2020). Existence of these modes is indicative of possible uses in applications such as fingerprint sensing (Tang et al., 2016; Jiang et al., 2017), chip-scale acoustic communication (Hoople et al., 2014; Kuo et al., 2014) *etc.* Moreover, appropriate design of the FeCAP waveguide and reflectors can generate high-frequency ultrasonic transducers for high resolution ultrasonic imaging (Bahr et al., 2019).

Conventional design topologies for integrated RF-MEMS oscillators using CMOS-MEMS resonators are not applicable owing to the small impedance of the intrinsic transduction capacitance C_0 in the devices at RF and mm-Wave operating frequencies. In order to obtain as large an output signal as possible from the device, its geometry is designed so as to maximize the capacitance C_0 . The large C_0 in-turn places limitations on the design of oscillation-sustaining circuitry and must therefore be compensated. It has been shown that for a 30 GHz RFT device having a Q-factor of 10,000 and motional resistance of 332 Ω , fundamental limits of oscillator phase noise (-132 dBc/Hz) can be achieved (Srivastava et al., 2021b) by using inductive compensation of the static capacitance C_0 . The inductor in this complementary cross-coupled oscillator topology is designed to resonate out the RFT static capacitance at the targeted resonance frequency. Similarly, active transistor sensing with an electromechanical transconductance $g_{m,mech}$ of $1 \mu\text{S}$ in the same 30 GHz RFT device can be utilized in a series feedback oscillator topology (Srivastava et al., 2021a). Alongside capacitive drive, inductive current-to-voltage conversion at the device output together with a tuned amplifier stage can be used to realize low phase noise oscillations. The resonant network of the tuned amplifier absorbs the large intrinsic device C_0 at the input. Using this oscillator topology, a figure-of-merit (FoM) of 228 dBc/Hz has been shown as being achievable with a phase noise of -140 dBc/Hz at 1 MHz offset from the oscillation frequency of 30 GHz. It is hence possible to achieve significantly better performance integrated oscillators as compared to purely LC based oscillators.

The devices and methods outlined here are the tip of the iceberg in terms of possibilities for seamless CMOS-MEMS integration. Exploitation of mechanical vibrations inside CMOS is currently limited by several factors, including incomplete characterization of individual thin film material properties within the CMOS stack, speed of design iteration and limited footprint for design optimization, computational costs of full 3D multiphysics simulation, and conservative design rules limiting lithographically-defined geometric optimization.

Particularly as CMOS foundries begin to launch ferroelectric materials within the transistor gate stack for memory and negative capacitance devices, there are exciting opportunities for CMOS-MEMS designers to work cooperatively with the foundry for short-loop, fast iteration, large-scale optimization across the full Design of Experiment. Joint efforts such as these promise new functionality to emerging technology platforms designed from the ground up. The designs and concepts discussed here can be translated to these modified platforms, opening doors for radio systems including tunable oscillators and switchable filter banks, novel nonlinear acoustic signal processing, oscillatory computation, and integrated sensor systems for IoT.

AUTHOR CONTRIBUTIONS

UR contributed to sections on phononic waveguide design, compact modeling, system design and applications as well as

introduction. JA contributed to the electromechanical conversion and introduction sections. This review was guided by DW.

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